National Semiconductor™

June 1997

PC87308VUL SuperI/O Enhanced Sidewinder Lite Plug and Play Compatible Chip, with a Floppy Disk Controller, a Keyboard Controller, a Real-Time Clock, Two UARTs, Full Infrared Support and an IEEE1284 Parallel Port

General Description

The PC87308VUL is a single-chip solution to the most commonly used ISA, EISA and MicroChannel® peripherals. This fully Plug and Play (PnP) compatible chip incorporates a Floppy Disk Controller (FDC), a Keyboard and mouse Controller (KBC), a Real-Time Clock (RTC), two full function UARTs, Infrared (IR) support, a full IEEE 1284 parallel port, three general purpose chip select signals that can be programmed for game port control, and a separate configuration register set for each module. It also provides support for power management and standard PC-AT address decoding for on-chip functions.

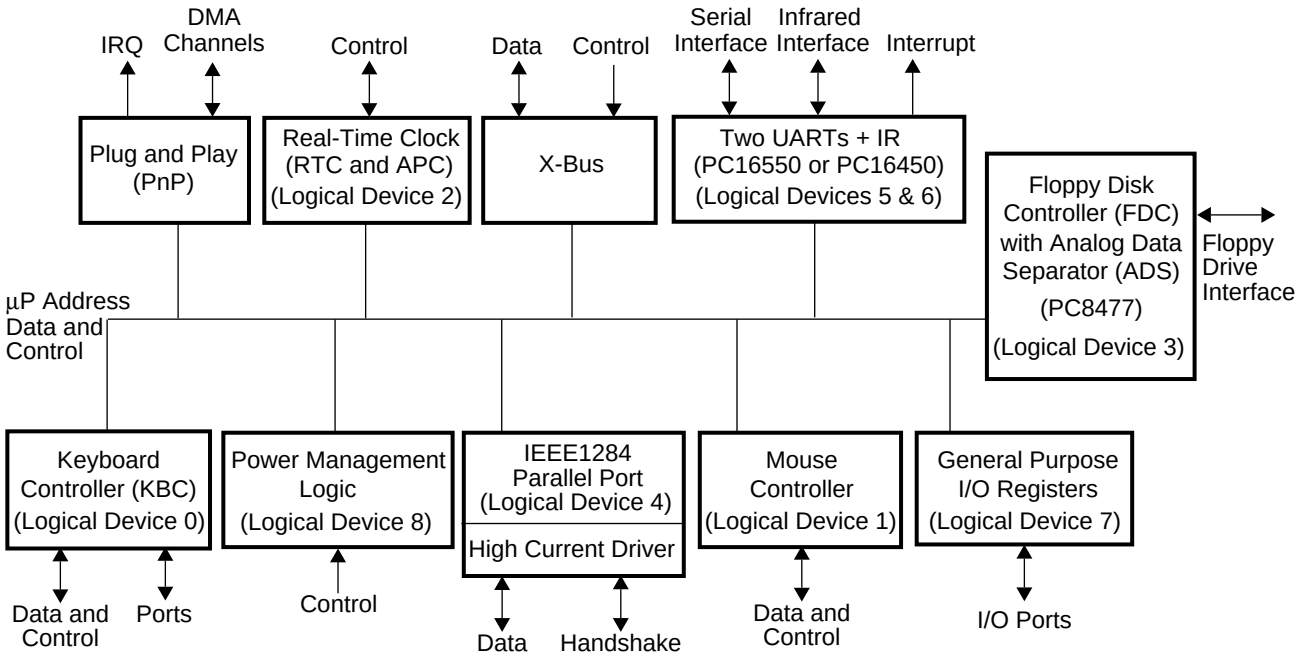
The Plug and Play (PnP) support in the PC87308VUL conforms to the "*Plug and Play ISA Specification*" Version 1.0a, May 5, 1994.

The Infrared (IR) interface complies with the IrDA 1.0 SIR, Sharp-IR and IrDA 1.1 standards, and supports all four basic protocols for Consumer-IR (TV remote) circuitry (RC-5, RC-5 extended, RECS80 and NEC).

Features

- 100% compatibility with Plug and Play requirements specified in the "*Plug and Play ISA Specification*", ISA, EISA, and MicroChannel architectures

Block Diagram



TRI-STATE® is a registered trademark of National Semiconductor Corporation.
IBM®, MicroChannel®, PC-AT® and PS/2® are registered trademarks of International Business Machines Corporation.
Microsoft® and Windows® are registered trademarks of Microsoft Corporation.

- A special Plug and Play (PnP) module that includes:
  - Flexible IRQs, DMAs and base addresses that meet the Plug and Play requirements specified by Microsoft® in their 1995 hardware design guide for Windows® and Plug and Play ISA Revision 1.0A
  - Plug and Play ISA mode (with isolation mechanism – Wait for Key state)
  - Motherboard Plug and Play mode
- A Floppy Disk Controller (FDC) that provides:
  - A modifiable address that is referenced by a 16-bit programmable register
  - Software compatibility with the PC8477, which contains a superset of the floppy disk controller functions in the µDP8473, the NEC µPD765A and the N82077
  - 13 IRQ channel options
  - Four 8-bit DMA channel options
  - 16-byte FIFO
  - Burst and non-burst modes
  - A high-performance, internal, analog data separator that does not require any external filter components
  - Support for standard 5.25" and 3.5" floppy disk drives
  - Automatic media sense support
  - Perpendicular recording drive support
  - Three-mode Floppy Disk Drive (FDD) support
  - Full support for the IBM Tape Drive Register (TDR) implementation of AT and PS/2 drive types
- A Keyboard and mouse Controller (KBC) with:
  - A modifiable address that is referenced by a 16-bit programmable register, reported as a fixed address in resource data
  - 13 IRQ options for the keyboard controller
  - 13 IRQ options for the mouse controller
  - An 8-bit microcontroller
  - Software compatibility with the 8042AH and PC87911 microcontrollers
  - 2 KB of custom-designed program ROM
  - 256 bytes of RAM for data
  - Five programmable dedicated open drain I/O lines for keyboard controller applications
  - Asynchronous access to two data registers and one status register during normal operation
  - Support for both interrupt and polling
  - 93 instructions
  - An 8-bit timer/counter
  - Support for binary and BCD arithmetic
  - Operation at 8 MHz,12 MHz or 16 MHz (programmable option)
  - Customizability using the PC87323VUL, which includes a RAM-based KBC, as a development platform for keyboard controller code for the PC87308VUL
- A Real-Time Clock (RTC) that has:
  - A modifiable address that is referenced by a 16-bit programmable register
  - 13 IRQ options, with programmable polarity
  - DS1287, MC146818 and PC87911 compatibility
  - 242 bytes of battery backed up CMOS RAM in two banks
  - Selective lock mechanism for the RTC RAM
  - Battery backed up century calendar in days, days of the week, months and years, with automatic leap-year adjustment
  - Battery backed-up time of day in seconds, minutes and hours that allows a 12 or 24 hour format and adjustments for daylight savings time
  - BCD or binary format for time keeping
  - Three different maskable interrupt flags:
    - Periodic interrupts - At intervals from 122 msec to 500 msec
    - Time-of-day alarm - At intervals from once per second to once per day
    - Updated Ended Interrupt - Once per second upon completion of update
  - Separate battery pin, 2.4 V operation that includes an internal UL protection resistor
  - 2 µA maximum power consumption during power down
  - Double-buffer time registers
- An Advanced Power supply Control (APC) that controls the main power supply to the system, using open-drain output, as follows:

  Power turned on when:
  - The RTC reaches a pre-determined date and time.
  - A high to low transition occurs on the $\overline{RI}$ input signals of the UARTs.
  - A ring pulse or pulse train is detected on the $\overline{RING}$ input signal.
  - A SWITCH input signal indicates a Switch On event

  Powered turned off when:
  - A SWITCH input signal indicates a Switch Off event
  - A Fail-safe event occurs (power-save mode detected but the system is hung up).
  - Software turns power off.
- Two UARTs that provide:
  - Software compatibility with the PC16550A and the PC16450
  - A modifiable address that is referenced by a 16-bit programmable register
  - 13 IRQ channel options
  - Shadow register support for write-only bits
  - Four 8-bit DMA options for UART2
- An Infrared (IR) interface on UART2 that supports Consumer-IR (TV-Remote) circuitry and is compliant with:
  - IrDA 1.1 MIR and FIR with 1.15 Mbps and 4 Mbps data rates
  - HP-SIR
  - ASK-IR option of SHARP-IR
  - DASK-IR option of SHARP-IR
- A bidirectional parallel port that includes:
  - A modifiable address that is referenced by a 16-bit programmable register
  - Software or hardware control

- — 13 IRQ channel options
- — Four 8-bit DMA channel options
- — Demand mode DMA support
- — An Enhanced Parallel Port (EPP) that is compatible with the new version EPP 1.9, and is IEEE1284 compliant
- — An Enhanced Parallel Port (EPP) that also supports version EPP 1.7 of the Xircom specification.
- — Support for an Enhanced Parallel Port (EPP) as mode 4 of the Extended Capabilities Port (ECP)
- — An Extended Capabilities Port (ECP) that is IEEE 1284 compliant, including level 2
- — Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
- — Reduction of PCI bus utilization by supporting a demand DMA mode mechanism and a DMA fairness mechanism
- — A protection circuit that prevents damage to the parallel port when a printer connected to it powers up or is operated at high voltages
- — Output buffers that can sink and source14 mA

■ Three general purpose pins for three separate programmable chip select signals, as follows:

- — Can be programmed for game port control
- — The Chip Select 0 ($\overline{CS0}$) signal produces open drain output and is powered by the V_{CCH}
- — The Chip Select 1 ($\overline{CS1}$) and 2 ($\overline{CS2}$) signals have push-pull buffers and are powered by the main V_{DD}
- — Decoding of chip select signals depends on the address and the Address Enable ($\overline{AEN}$) signals, and can be qualified using the Read ($\overline{RD}$) and Write ($\overline{WR}$) signals.

■ 16 single-bit General Purpose I/O ports (GPIO):

- — Modifiable addresses that are referenced by a 16-bit programmable register
- — Programmable direction for each signal (input or output)
- — Programmable drive type for each output pin (open-drain or push-pull)
- — Programmable option for internal pull-up resistor on each input pin
- — A back-drive protection circuit

■ An X-bus data buffer that connects the 8-bit X data bus to the ISA data bus

■ Clock source options:

- — Source is a 32.768 KHz crystal - an internal frequency multiplier generates all the required internal frequencies.
- — Source may be either a 48 MHz or 24 MHz clock input signal.

■ Enhanced Power Management (PM), including:

- — Special configuration registers for power down
- — Reduced current leakage from pins
- — Low-power CMOS technology
- — Ability to shut off clocks to all modules

■ General features include:

- — All accesses to the SuperI/O chip activate a Zero Wait State ($\overline{ZWS}$) signal, except for accesses to the Enhanced Parallel Port (EPP) and to configuration registers
- — Access to all configuration registers is through an Index and a Data register, which can be relocated within the ISA I/O address space
- — 160-pin Plastic Quad Flatpack (PQFP) package

Basic Configuration

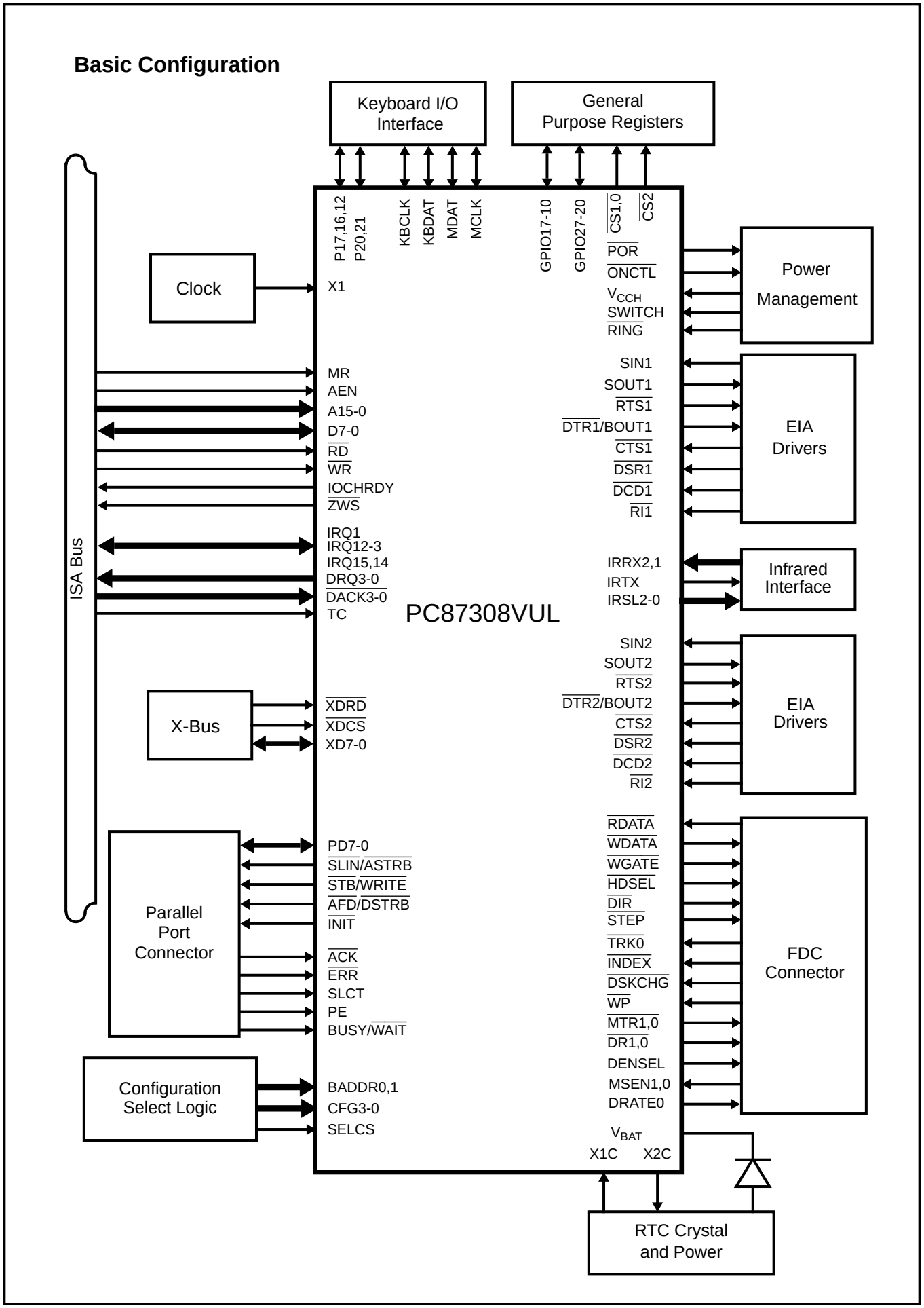


Table of Contents

7.0 UART1 and UART2 (with Fast IR) (Logical Devices 6 and 5)

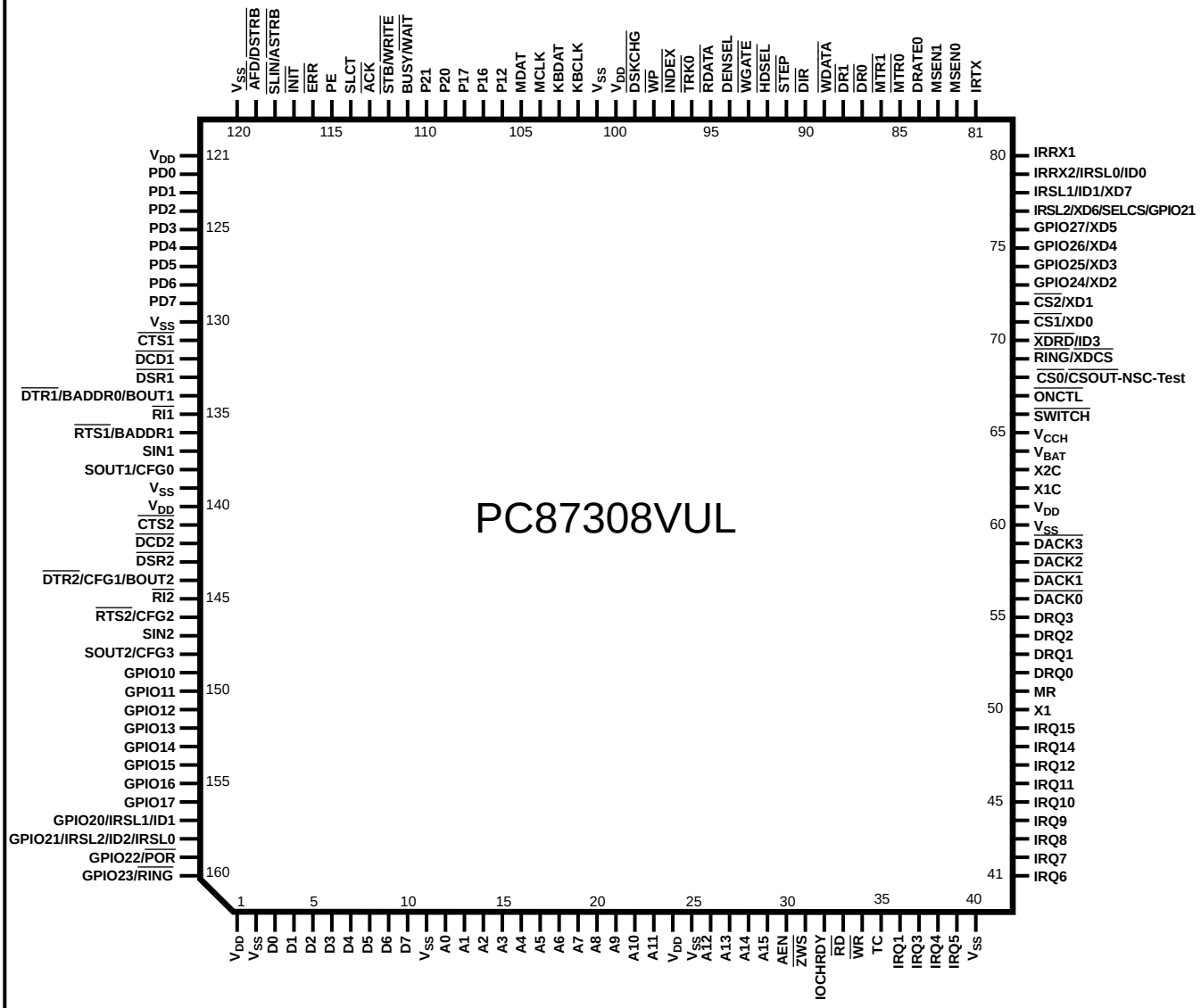
List of Figures

List of Tables

1.0 Signal/Pin Connection and Description

1.1 CONNECTION DIAGRAM

PlasticQuad Flatpack (PQFP), EIAJ



Order Number PC87308VUL
See NS Package Number VUL160A

1.2 SIGNAL/PIN DESCRIPTIONS

Table 1-1 lists the signals of the PC87308VUL in alphabetical order and shows the pin(s) associated with each. Table 1-2 on page 10 lists the X-Bus Data Buffer (XDB) signals that are multiplexed and Table 1-3 on page 10 lists the pins that have strap functions during reset.

The Module column indicates the functional module that is associated with these pins. In this column, the System label indicates internal functions that are common to more than one module.

The I/O and Group # column describes whether the pin is an input, output, or bidirectional pin (marked as Input, Output or I/O, respectively). This column also specifies the DC characteristics group to which this pin belongs. See Section 13.2 on page 166 for details.

Refer to the glossary for an explanation of abbreviations and terms used in this table, and throughout this document. Use the Table of Contents to find more information about each register.

TABLE 1-1. Signal/Pin Description Table

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
A15-0	29-26, 23-12	ISA-Bus	Input Group 1	**ISA-Bus Address –** A15-0 are used for address decoding on any access except DMA accesses, on the condition that the AEN signal is low. See Address Decoding in Section 2.2.2 on page 12.
$\overline{\text{ACK}}$	113	Parallel Port	Input Group 3	**Acknowledge –** This input signal is pulsed low by the printer to indicate that it has received data from the parallel port. It is pulled up by an internal nominal 25 KΩ pull-up resistor.
$\overline{\text{AFD}}$	119	Parallel Port	I/O Group 13	**Automatic Feed –** When this signal is low the printer should automatically feed a line after printing each line. This pin is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be attached to this pin. For Input mode see bit 5 in “Control0, Second Level Offset 00h” on page 99. This pin is multiplexed with $\overline{\text{DSTRB}}$. See $\overline{\text{DSTRB}}$ and Table 6-12 on page 107 for more information.
AEN	30	ISA-Bus	Input Group 1	**DMA Address Enable –** This input signal disables function selection via A15-A0 when it is high. Access during DMA transfer is not affected by this signal.
$\overline{\text{ASTRB}}$	118	Parallel Port	Output Group 4	**Address Strobe (EPP) –** This signal is used in EPP mode as address strobe. It is active low. This pin is multiplexed with $\overline{\text{SLIN}}$. See Table 6-12 on page 107 for more information.
BADDR1,0	136, 134	Configuration	Input Group 5	**Base Address Strap Pins 0 and 1 –** These pins determine the base addresses of the Index and Data registers, the value of the Plug and Play ISA Serial Identifier and the configuration state immediately after reset. These pins are pulled down by internal 30 KΩ resistors. External 10 KΩ pull-up resistors to V_{DD} should be employed. BADDR1 is multiplexed with $\overline{\text{RTS1}}$. BADDR0 is multiplexed with $\overline{\text{DTR1}}$ and BOUT1. See Table 2-2 on page 12 and Section 2.1 on page 11.
BOUT2,1	144, 134	UART1, UIR	Output Group 17	**Baud Output –** This multi-function pin provides the associated serial channel Baud Rate generator output signal if test mode is selected, i.e., bit 7 of the EXCR1 register is set. (See Section 7.15.2 on page 130.) BOUT2 is multiplexed with $\overline{\text{DTR2}}$ and CFG1. BOUT1 is multiplexed with $\overline{\text{DTR1}}$ and BADDR0.
BUSY	111	Parallel Port	Input Group 2	**Busy –** This pin is set high by the printer when it cannot accept another character. It is internally connected to a nominal 25 KΩ pull-down resistor. This pin is multiplexed with $\overline{\text{WAIT}}$. See Table 6-12 on page 107 for more information.

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
CFG3-0	148, 146, 144, 138	Configuration	Input Group 5	**Configuration Strap Pins 3-0 –** These pins determine the default configuration upon power up. These pins are pulled down by internal 30 KΩ resistors. External 10 KΩ pull-up resistors to V_{DD} should be employed. CFG3 is multiplexed with SOUT2. CFG2 is multiplexed with $\overline{RTS2}$. CFG1 is multiplexed with $\overline{DTR2}$ and BOUT2. CFG0 is multiplexed with SOUT1. See Table 2-2 on page 12 and Section 2.1 on page 11.
$\overline{CS0}$	68	General Purpose	Output Group 21	**Programmable Chip Select –** $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$ are programmable chip select and/or latch enable and/or output enable signals that have many uses, for example, as game ports or for I/O port expansion. The decoded address and the assertion conditions are configured via the PC87308VUL's configuration registers. See Section 2.3 on page 13. $\overline{CS0}$ is an open-drain pin that is in TRI-STATE unless V_{DD} is applied. $\overline{CS2}$ is multiplexed with XD1, $\overline{CS1}$ is multiplexed with XD0, and $\overline{CS0}$ is multiplexed with $\overline{CSOUT}$-NSC-Test.
$\overline{CS2,1}$	72, 71	General Purpose	I/O Group 9	
$\overline{CSOUT}$-NSC-Test	68	NSC-use	Output Group 21	**Chip Select Read Output, NSC-Test –** This National Semiconductor test signal is an open-drain output signal. This signal is multiplexed with $\overline{CS0}$.
$\overline{CTS2,1}$	141, 131	UART1, UIR	Input Group 1	**UART1 and UIR Clear to Send –** When low, these signals indicate that the modem or other data transfer device is ready to exchange data. The $\overline{CTS}$ signal is a modem status input signal whose condition the CPU can test by reading bit 4 (CTS) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of MSR indicates whether the $\overline{CTS}$ input signal has changed state since the previous reading of MSR. $\overline{CTS}$ has no effect on the transmitter. Whenever the DCTS bit of the MSR is set, an interrupt is generated if modem status interrupts are enabled.
D7-0	10-3	ISA-Bus	I/O Group 8	**ISA-Bus Data -** Bidirectional data lines to the microprocessor. D0 is the LSB and D7 is the MSB. These signals have 24 mA (sink) buffered outputs.
$\overline{DACK3-0}$	59-56	ISA-Bus	Input Group 1	**DMA Acknowledge 0,1,2 and 3 –** These active low input signals acknowledge a request for DMA services and enable the $\overline{IOWR}$ and $\overline{IORD}$ input signals during a DMA transfer. These DMA signals can be mapped to the following logical devices: FDC, UART1, UIR or parallel port.
$\overline{DCD2,1}$	142, 132	UART1, UIR	Input Group 1	**UART1 and UIR Data Carrier Detected –** When low, this signal indicates that the modem or other data transfer device has detected the data carrier. The $\overline{DCD}$ signal is a modem status input signal whose condition the CPU can test by reading bit 7 (DCD) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the MSR indicates whether the $\overline{DCD}$ input signal has changed state since the previous reading of MSR. Whenever the DDCD bit of the MSR is set, an interrupt is generated if modem status interrupts are enabled.
DENSEL	94	FDC	Output Group 16	**Density Select (FDC) –** Indicates that a high FDC density data rate (500 Kbps or 1 Mbps) or a low density data rate (250 or 300 Kbps) is selected. DENSELs polarity is controlled by bit 5 of the SuperI/O FDC Configuration register as described in Section 2.6.1 on page 23.

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
$\overline{\text{DIR}}$	90	FDC	Output Group 16	**Direction (FDC) –** This output signal determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in, inactive = step out) during a seek operation. During reads or writes, $\overline{\text{DIR}}$ is inactive.
$\overline{\text{DR1,0}}$	88, 87	FDC	Output Group 16	**Drive Select 0 and 1 (FDC) –** These active low output signals are the decoded drive select output signals. $\overline{\text{DR0}}$ and $\overline{\text{DR1}}$ are controlled by Digital Output Register (DOR) bits 0 and 1. They are encoded with information to control four FDDs when bit 7 of the SuperI/O FDC Configuration register is 1, as described in Section 2.6.1 on page 23. See $\overline{\text{MTR0,1}}$ for more information.
DRATE0	84	FDC	Output Group 20	**Data Rate 0 (FDC) –** This output signal reflects the currently selected FDC data rate, (bits 0 and 1 in the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last. Output from the pin is totem-pole buffered (6 mA sink, 6 mA source).
DRQ3-0	55-52	ISA-Bus	Output Group 18	**DMA Request 0, 1, 2 and 3 –** These active high output signals inform the DMA controller that a data transfer is needed. These DMA signals can be mapped to the following logical devices: Floppy Disk Controller (FDC), UART1, UIR or parallel port.
$\overline{\text{DSKCHG}}$	99	FDC	Input Group 1	**Disk Change (FDC) –** This input signal indicates whether or not the drive door has been opened. The state of this pin is available from the Digital Input Register (DIR). This pin can also be configured as the RGATE data separator diagnostic input signal via the MODE command. See the MODE command in Section 5.3.2 starting on page 71.
$\overline{\text{DSR2,1}}$	143, 133	UART1, UIR	Input Group 1	**Data Set Ready –** When low, this signal indicates that the data transfer device, e.g., modem, is ready to establish a communications link. The $\overline{\text{DSR}}$ signal is a modem status input signal whose condition the CPU can test by reading bit 5 (DSR) of the Modem Status Register (MSR) for the appropriate channel. Bit 5 is the complement of the $\overline{\text{DSR}}$ signal. Bit 1 (DDSR) of the MSR indicates whether the $\overline{\text{DSR}}$ input signal has changed state since the previous reading of the MSR. Whenever the DDSR bit of the MSR is set, an interrupt is generated if modem status interrupts are enabled.
$\overline{\text{DSTRB}}$	119	Parallel Port	Output Group 23	**Data Strobe (EPP) –** This signal is used in EPP mode as a data strobe. It is active low. $\overline{\text{DSTRB}}$ is multiplexed with $\overline{\text{AFD}}$. See Table 6-12 on page 107 for more information.
$\overline{\text{DTR2,1}}$	144, 134	UART1, UIR	Output Group 17	**Data Terminal Ready –** When low, this output signal indicates to the modem or other data transfer device that the UART1 or UIR is ready to establish a communications link. The $\overline{\text{DTR}}$ signal can be set active low by programming bit 0 (DTR) of the Modem Control Register (MCR) to high (1). A Master Reset (MR) deactivates this signal high, and loopback operation holds this signal inactive. $\overline{\text{DTR2}}$ is multiplexed with CFG1 and BOUT2. $\overline{\text{DTR1}}$ is multiplexed with BADDR0 and BOUT1.
$\overline{\text{ERR}}$	116	Parallel Port	Input Group 3	**Error –** This input signal is set active low by the printer when it has detected an error. This pin is internally connected to a nominal 25 KΩ pull-up resistor.
GPIO17-10	156-149	General Purpose	I/O Group 10	**General Purpose I/O Signals 17-10 –** General purpose I/O signals of I/O Port 1.

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
GPIO20 GPIO21 GPIO22 GPIO23 GPIO27-24	157 77, 158 159 160 76-73	General Purpose	I/O Group 10	**General Purpose I/O Signals 27-20 –** General purpose I/O port 2 signals. GPIO27-24 are multiplexed with XD5-2, respectively. GPIO23 is multiplexed with $\overline{\text{RING}}$. GPIO 22 is multiplexed with $\overline{\text{POR}}$. GPIO 21 is multiplexed on pin 158 with IRSL2, IRSL0 and ID2 and on pin 77 with IRSL2, SELCS and XD6. See "SuperI/O Configuration 2 Register, Index 22h" on page 22. GPIO20 is multiplexed with IRSL1 and ID1.
$\overline{\text{HDSEL}}$	92	FDC	Output Group 16	**Head Select –** This output signal determines which side of the FDD is accessed. Active low selects side 1, inactive selects side 0.
ID0 ID1 ID2 ID3	79 78 or 157 158 70	UART2	Input Group 1	**Identification –** These ID signals identify the infrared transceiver for Plug and Play support. These pins are read after reset. ID0 is multiplexed on pin 79 with IRRX2 and IRSL0. ID1 is multiplexed on pin 78 with IRSL1 and XD7, or on pin 157 with GPIO20 and IRSL1. ID2 is multiplexed on pin 158 with GPIO21, IRSL2 and IRSL0. ID3 is multiplexed on pin 70 with $\overline{\text{XDRD}}$. See Table 1-2 on page 10 for more information.
$\overline{\text{INDEX}}$	97	FDC	Input Group 1	**Index –** This input signal indicates the beginning of an FDD track.
$\overline{\text{INIT}}$	117	Parallel Port	I/O Group 13	**Initialize –** When this signal is active low, it causes the printer to be initialized. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be employed.
IOCHRDY	32	ISA-Bus	Output Group 22	**I/O Channel Ready –** This is the I/O channel ready open drain output signal. When IOCHRDY is driven low, the EPP extends the host cycle.
IRQ1 IRQ5-3 IRQ12-6 IRQ15,14	36 39-37 47-41 49,48	ISA-Bus	I/O Group 15	**Interrupt Requests 1, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14 and 15 –** IRQ polarity and push-pull or open-drain output selection is software configurable by the logical device mapped to the IRQ line. Keyboard Controller (KBC) or Mouse interrupts can be configured by the Interrupt Request Type Select 0 register (index 71h) as either edge or level. The parallel port interrupt is either edge or level, according to the operation mode (default edge, configured by the SuperI/O Parallel Port Configuration register at index F0h).
IRRX2,1	79, 80	UIR	Input Group 1	**Infrared Reception 1 and 2 –** Infrared serial input data. IRRX2 is multiplexed with IRSL0 and ID0. See Table 1-2 on page 10 for more information.
IRSL0 IRSL1 IRSL2	79 or 158 78 or 157 77 or 158 77, 78, 79 157, 158	UIR	Output Group 17 Group 10	**Infrared Control Signals 0, 1 and 2 –** These signals control the Infrared analog front end. The pins on which these signals are driven is determined by the SuperI/O Configuration 2 register (index 22h). See Section 2.4.2 on page 22. IRSL0 on pin 79 is determined by UART2 bit 5 of the register at offset 07h in bank 7 (See Section 7.20.8). IRSL0 is multiplexed on pin 79 with IRRX2 and ID0, or on pin 158 with GPIO21, IRSL2 and ID2 . IRSL1 is multiplexed on pin 78 with XD7 and ID1, or on pin 157 with GPIO20 and ID1. IRSL2 is multiplexed on pin 77 with XD6, SELCS and GPIO21, or on pin 158 with GPIO21, IRSL0 and ID2.

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
IRTX	81	UIR	Output Group 19	**Infrared Transmit –** Infrared serial output data.
KBCLK	102	KBC	I/O Group 11	**Keyboard Clock –** This I/O pin transfers the keyboard clock between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is connected internally to the T0 signal of the KBC.
KBDAT	103	KBC	I/O Group 11	**Keyboard Data –** This I/O pin transfers the keyboard data between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is connected internally to the P10 signal of the KBC.
MCLK	104	KBC	I/O Group 11	**Mouse Clock –** This I/O pin transfers the mouse clock between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is connected internally to the T1 signal of the KBC.
MDAT	105	KBC	I/O Group 11	**Mouse Data –** This I/O pin transfers the mouse data between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is connected internally to the P11 signal of the KBC.
MR	51	ISA-Bus	Input Group 1	**Master Reset –** An active high MR input signal resets the controller to the idle state, and resets all disk interface output signals to their inactive states. MR also clears the DOR, DSR and CCR registers, and resets the MODE command, CONFIGURE command, and LOCK command parameters to their default values. MR does not affect the SPECIFY command parameters. MR sets the configuration registers to their selected default values.
MSEN1,0	83, 82	FDC	Input Group 4	**Media Sense –** These input pins are used for media sensing when bit 6 of the SuperI/O FDC Configuration register (at index F0h) is 1. See Section 2.6.1 on page 23. Each pin has a 40 KΩ internal pull-up resistor.
$\overline{\text{MTR1,0}}$	86, 85	FDC	Output Group 16	**Motor Select 1,0 –** These motor enable lines for drives 0 and 1 are controlled by bits D7-4 of the Digital Output Register (DOR). They are output signals that are active when they are low. They are encoded with information to control four FDDs when bit 7 of the SuperI/O FDC Configuration register is set, as described in Section 2.6.1 on page 23. See $\overline{\text{DR1,0}}$.
$\overline{\text{ONCTL}}$	67	APC	Output Group 23	**On/Off Control for the RTC's Advanced Power Control (APC) –** This signal indicates to the main power supply that power should be turned on. $\overline{\text{ONCTL}}$ is an open-drain output signal that is powered by V_{CCH}.
P17,16 P12	108, 107 106	KBC	I/O Group 12	**I/O Port –** KBC quasi-bidirectional port for general purpose input and output.
P21,20	110,109	KBC	I/O Group 12	**I/O Port –** KBC open-drain signals for general purpose input and output. These signals are controlled by KBC firmware.
PD7-0	129-122	Parallel Port	I/O Group 14	**Parallel Port Data –** These bidirectional signals transfer data to and from the peripheral data bus and the appropriate parallel port data register. These signals have a high current drive capability. See "GENERAL DC ELECTRICAL CHARACTERISTICS" on page 165.
PE	115	Parallel Port	Input Group 2	**Paper End –** This input signal is set high by the printer when it is out of paper. This pin has an internal nominal 25 KΩ pull-up or pull-down resistor that is selected by bit 2 of the PP Confg0 register (second level offset 05h) of the parallel port.

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
$\overline{POR}$	159	APC	Output Group 21	**Power Off Request –** This signal becomes active when an APC Switch Off event occurs, regardless of the fail-safe delay. Selection of edge or level for $\overline{POR}$ is via the APCR1 register of the APC. Selection of an output buffer is via GPIO22 output buffer control bits (in the Port 2 Output Type and Port 2 Pull-up Control registers described in Table 8-1 on page 156). See Section 4.3 on page 41. This signal is multiplexed with GPIO22.
$\overline{RD}$	33	ISA-Bus	Input Group 1	**I/O Read –** An active low $\overline{RD}$ input signal indicates that the microprocessor has read data.
$\overline{RDATA}$	95	FDC	Input Group 1	**Read Data –** This input signal holds raw serial data read from the Floppy Disk Drive (FDD).
$\overline{RI2,1}$	145, 135	UART1, APC	Input Group 7	**Ring Indicators (Modem) –** When low, this signal indicates that a telephone ring signal has been received by the modem. The CPU can test the status of the $\overline{RI}$ modem status input signal by reading bit 6 (RI) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MSR indicates whether the $\overline{RI}$ input signal has changed from low to high since the previous reading of the MSR. When the TERI bit of the MSR is set, an interrupt is generated if modem status interrupts are enabled. When enabled, a high to low transition on $\overline{RI1}$ or $\overline{RI2}$ activates the $\overline{ONCTL}$ pin. The RI1 and RI2 pins each have an schmitt-trigger input buffer.
$\overline{RING}$	69 or 160	APC	Input Group 7	**Ring Indicator (APC) –** Detection of an active low $\overline{RING}$ pulse or pulse train activates the $\overline{ONCTL}$ signal. The APC's APCR2 register determines which pin the $\overline{RING}$ signal uses. The pins have a schmitt-trigger input buffer. $\overline{RING}$ is multiplexed on pin 69 with $\overline{XDCS}$ and on pin 160 with GPIO23.
$\overline{RTS2,1}$	146, 136	UART1, UIR	Output Group 17	**Request to Send –** When low, these output signals indicate to the modem or other data transfer device that the corresponding UART is ready to exchange data. The $\overline{RTS}$ signal can be set active low by programming bit 1 (RTS) of the Modem Control Register (MCR) to a high level. A Master Reset (MR) sets $\overline{RTS}$ to inactive high. Loopback operation holds it inactive. $\overline{RTS2}$ is multiplexed with CFG2. $\overline{RTS1}$ is multiplexed with BADDR1.
SELCS	77	Configuration	Input Group 4	**Select CSOUT –** During reset, this signal is sampled into bit 1 of the SuperI/O Configuration 1 register (index 21h). A 40 KΩ internal pull-up resistor (or a 10 KΩ external pull-down resistor for National Semiconductor testing) controls this pin during reset. Do not pull this signal low during reset. This signal is multiplexed with IRSL2, GPIO21 and XD6. See Table 1-2 on page 10.
SIN2,1	147, 137	UART1, UIR	Input Group 1	**Serial Input –** This input signal receives composite serial data from the communications link (peripheral device, modem or other data transfer device.)
SLCT	114	Parallel Port	Input Group 2	**Select –** This input signal is set active high by the printer when the printer is selected. This pin is internally connected to a nominal 25 KΩ pull-down resistor.
$\overline{SLIN}$	118	Parallel Port	I/O Group 13	**Select Input –** When this signal is active low it selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be employed. This signal is multiplexed with $\overline{ASTRB}$.

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
SOUT2,1	148, 138	UART1, UIR	Output Group 17	**Serial Output –** This output signal sends composite serial data to the communications link (peripheral device, modem or other data transfer device). The SOUT2,1 signals are set active high after a Master Reset (MR). SOUT2 is multiplexed with CFG3. SOUT1 is multiplexed with CFG0.
$\overline{STB}$	112	Parallel Port	I/O Group 13	**Data Strobe –** This output signal indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be employed. This signal is multiplexed wiTH $\overline{WRITE}$.
$\overline{STEP}$	91	FDC	Output Group 16	**Step –** This output signal issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
$\overline{SWITCH}$	66	APC	Input Group 7	**Switch On/Off –** Indicates a request to the APC to switch the power on or off. When V_{DD} does not exist, a high to low transition on this signal indicates a Switch On request. When V_{DD} exists, a high to low transition on this pin indicates a Switch Off request. The pin has an internal pull-up of 1 MΩ (nominal), a schmitt-trigger input buffer and debounce protection of at least 16 msec.
TC	35	ISA-Bus	Input Group 1	**DMA Terminal Count –** The DMA controller issues TC to indicate the termination of a DMA transfer. TC is accepted only when a $\overline{DACK}$ signal is active. TC is active high in PC-AT mode, and active low in PS/2 mode.
$\overline{TRK0}$	96	FDC	Input Group 1	**Track 0 –** This input signal indicates to the controller that the head of the selected floppy disk drive is at track 0.
V_{BAT}	64	RTC and APC	Input	**Battery Power Supply –** Power signal from the battery to the Real-Time Clock (RTC) or for Advanced Power Control (APC) when V_{CCH} is less than V_{BAT} (by at least 0.5 V). V_{BAT} includes a UL protection resistor.
V_{CCH}	65	RTC and APC	Input	**V_{CC} Help Power Supply –** This signal provides power to the RTC or APC when V_{CCH} is higher than V_{BAT} (by at least 0.5 V).
V_{DD}	1, 24, 61, 100, 121, 140	Power Supply	Input	**Main 5 V Power Supply –** This signal is the 5 V supply voltage for the digital circuitry.
V_{SS}	2, 11, 25, 40, 60, 101, 120, 130, 139	Power Supply	Output	**Ground –** This signal provides the ground for the digital circuitry.
$\overline{WAIT}$	111	Parallel Port	Input Group 2	**Wait –** In EPP mode, the parallel port device uses this signal to extend its access cycle. $\overline{WAIT}$ is active low. This signal is multiplexed with BUSY. See Table 6-12 on page 107 for more information.
$\overline{WDATA}$	89	FDC	Output Group 16	**Write Data (FDC) –** This output signal holds the write precompensated serial data that is written to the selected floppy disk drive. Precompensation is software selectable.
$\overline{WGATE}$	93	FDC	Output Group 16	**Write Gate (FDC) –** This output signal enables the write circuitry of the selected disk drive. $\overline{WGATE}$ is designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled.

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
$\overline{WP}$	98	FDC	Input Group 1	**Write Protected –** This input signal indicates that the disk in the selected drive is write protected.
$\overline{WR}$	34	ISA-Bus	Input Group 1	**I/O Write –** $\overline{WR}$ is an active low input signal that indicates a write operation from the microprocessor to the controller.
$\overline{WRITE}$	112	Parallel Port	Output Group 23	**Write Strobe –** In EPP mode, this active low signal is a write strobe. This signal is multiplexed with $\overline{STB}$. See Table 6-12 on page 107 for more information.
X1	50	Clock	Input Group 6	**Clock In –** A TTL or CMOS compatible 24 MHz or 48 MHz clock. See Chapter 11.
X1C	62	RTC	Input	**Crystal 1 Slow –** Input signal to the internal Real-Time Clock (RTC) crystal oscillator amplifier.
X2C	63	RTC	Output	**Crystal 2 Slow –** Output signal from the internal Real-Time Clock (RTC) crystal oscillator amplifier.
XD7,6 XD1,0	78,77 72,71	X-Bus	I/O Group 9	**X-Bus Data –** These bidirectional signals hold the data in the X Data Buffer (XDB). XD7 is multiplexed with IRSL1 and ID1. XD6 is multiplexed with IRSL2 and SELCS. XD5-2 are multiplexed with GPIO27-24, respectively. XD1,0 are multiplexed with $\overline{CS2,1}$ respectively. See Table 1-2.
XD5-2	76-73		I/O Group 10	
$\overline{XDCS}$	69	X-Bus	Input Group 7	**X-Bus Data Buffer (XDB) Chip Select –** This signal enables and disables the bidirectional XD7-0 data buffer signals. This signal is multiplexed with $\overline{RING}$. See Table 1-2.
$\overline{XDRD}$	70	X-Bus	Input Group 1	**X-Bus Data Buffer (XDB) Read Command –** This signal controls the direction of the bidirectional XD7-0 data buffer signals.
$\overline{ZWS}$	31	ISA-Bus	Output Group 22	**Zero Wait State –** When this open-drain output signal is activated (driven low), it indicates that the access time can be shortened, i.e., zero wait states. $\overline{ZWS}$ is never activated (driven low) on access to SuperI/O chip configuration registers (including during the Isolation state) or on access to the parallel port in SPP or EPP 1.9 mode. $\overline{ZWS}$ is always activated (driven low) on access to the parallel port in ECP mode. Assertion of $\overline{ZWS}$ on access to a parallel port in EPP 1.7 mode is controlled by bit 3 of the Control2 register (at second level offset 02h) of the parallel port (accessed by the Index and Data registers at base+403h and base+404h). See page 100. Bit 0 of the SuperI/O Configuration 1 register (at index 21h) controls assertion of $\overline{ZWS}$ on access to any other addresses of the PC87308VUL. See page 21.

In Table 1-2, unselected (XDB or alternate function) input signals are internally blocked high.

TABLE 1-2. Multiplexed X-Bus Data Buffer (XDB) Pins

Pin	X-Bus Data Buffer (XDB) Bit 4 of SuperI/O Configuration Register 1 = 1	I/O	Alternate Function Bit 4 of SuperI/O Configuration 1 Register = 0	I/O
69	$\overline{\text{XDCS}}$	Input	$\overline{\text{RING}}$	Input
70	$\overline{\text{XDRD}}$	Input	ID3	Input
71	XD0	I/O	$\overline{\text{CS1}}$	Output
72	XD1	I/O	$\overline{\text{CS2}}$	Output
73	XD2	I/O	GPIO24	I/O
73	XD3	I/O	GPIO25	I/O
75	XD4	I/O	GPIO26	I/O
76	XD5	I/O	GPIO27	I/O
77	XD6/SELCS	I/O	IRSL2/SELCS/GPIO21	I/O
78	XD7	I/O	IRSL1/ID1	I/O

TABLE 1-3. Pins with a Strap Function During Reset

Strap Pins	Pin Number	Pin Symbols
BADDR1,0	134	$\overline{\text{DTR1}}$/BADDR0/BOUT1
	136	$\overline{\text{RTS1}}$/BADDR1
CFG3-0	138	SOUT1/CFG0
	144	$\overline{\text{DTR2}}$/CFG1/BOUT2
	146	$\overline{\text{RTS2}}$/CFG2
	148	SOUT2/CFG3
SELCS	77	IRSL2//XD6/SELCS/GPIO21

2.0 Configuration

The PC87308VUL is partially configured by hardware, during reset. The configuration can also be changed by software, by changing the values of the configuration registers.

The configuration registers are accessed using an Index register and a Data register. During reset, hardware strapping options define the addresses of the configuration registers. See Section 2.1.2.

After the Index and Data register pair have determined the addresses of the configuration registers, the addresses of the Index and Data registers can be changed within the ISA I/O address space, and a 16-bit programmable register controls references to their addresses and to the addresses of the other registers.

This chapter describes the hardware and software configuration processes. For each, it describes configuration of the Index and Data register pair first. See Sections 2.1 and 2.2.

Section 2.3 starting on page 13 presents an overview of the configuration registers of the PC87308VUL and describes each in detail.

2.1 HARDWARE CONFIGURATION

The PC87308VUL supports two Plug and Play (PnP) configuration modes that determine the status of register addresses upon wake up from a hardware reset, Full Plug and Play ISA mode and Plug and Play Motherboard mode.

2.1.1 Wake Up Options

During reset, strapping options on the BADDR0 and BADDR1 pins determine one of the following modes.

- Full Plug and Play ISA mode – System wakes up in Wait for Key state.

  Index and Data register addresses are as defined by Microsoft and Intel in the *"Plug and Play ISA Specification, Version 1.0a, May 5, 1994."*

- Plug and Play Motherboard mode – System wakes up in Config state.

  The BIOS configures the PC87308VUL. Index and Data register addresses are different from the addresses of the Plug and Play (PnP) Index and Data registers. Configuration registers can be accessed as if the serial isolation procedure had already been done, and the PC87308VUL is selected.

  The BIOS may switch the addresses of the Index and Data registers to the PnP ISA addresses of the Index and Data registers, by using software to modify the base address bits of the SuperI/O Configuration 2 register (at Index 22h). See Section 2.4.2

2.1.2 The Index and Data Register Pair

During reset, a hardware strapping option on the BADDR0 and BADDR1 pins defines an address for the Index and Data Register pair. This prevents contention between the registers for I/O address space.

Table 2-1 shows the base addresses for the Index and Data registers that hardware sets for each combination of values of the Base Address strap pins (BADDR0 and BADDR1). You can access and change the content of the configuration registers at any time, as long as the base addresses of the Index and Data registers are defined.

When BADDR1 is low (0), the Plug and Play (PnP) protocol defines the addresses of the Index and Data register, and the system wakes up from reset in the Wait for Key state.

When BADDR1 is high (1), the addresses of the Index and Data register are according to Table 2-1, and the system wakes up from reset in the Config state.

This configures the PC87308VUL with default values, automatically, without software intervention. After reset, use software as described in Section 2.2 to modify the selected base address of the Index and Data register pair, and the defaults for configuration registers.

The Plug and Play soft reset has no effect on the logical devices, except for the effect of the Activate registers (index 30h) in each logical device.

The PC87308VUL can wake up with the FDC, the KBC and the RTC either active (enabled) or inactive (disabled). The clock multiplier, if configured via CFG3,2 strap pins, wakes up enabled. The other logical devices wake up inactive (disabled).

TABLE 2-1. Base Addresses

BADDR1	BADDR0	Address		Configuration Type
		Index Register	Data Register	
0	x	0279h Write Only	Write: 0A79h Read: RD_DATA Port	Full PnP ISA Mode Wake up in Wait for Key state
1	0	015Ch Read/Write	015Dh Read/Write	PnP Motherboard Mode Wake up in Config state
1	1	002Eh Read/Write	002Fh Read/Write	PnP Motherboard Mode Wake up in Config state

2.1.3 The Strap Pins

TABLE 2-2. The Strap Pins

Pin	Reset Configuration	Affected
CFG0	0 - FDC, KBC and RTC wake up inactive. 1 - FDC, KBC and RTC wake up active.	Bit 0 of Activate registers (index 30h) of logical devices 0,2 and 3.
CFG1	0 - No X-Bus Data Buffer. (See XDB pins multiplexing in Table 1-2.) 1 - X-Bus Data Buffer (XDB) enabled.	Bit 4 of SuperI/O Configuration 1 register (index 21h).
CFG3,2	00 - Clock source is 24 MHz fed via X1 pin. 01 - Reserved for $\overline{\text{CSOUT}}$-NSC-Test fed via X1 pin. 10 - Clock source is 48 MHz fed via X1 pin. 11 - Clock source is 32.768 KHz with on-chip clock multiplier.	Bits 2-0 of PMC2 register of Power Management (logical device 8) CFG2 affects bits 0 and 2. CFG3 affects bit 1.
BADDR1,0	00 - Full PnP ISA, Wake in Wait For Key state. Index PnP ISA. 01 - Full PnP ISA, Wake in Wait For Key state. Index PnP ISA. 10 - PnP Motherboard, Wake in Config state. Index 015Ch. 11 - PnP Motherboard, Wake in Config state. Index 002Eh.	Bits 1 and 0 of SuperI/O Configuration 2 register (index 22h).
SELCS	0 - $\overline{\text{CSOUT}}$-NSC-test on $\overline{\text{CS0}}$ pin. 1 - $\overline{\text{CS0}}$ on $\overline{\text{CS0}}$ pin.	Bit 1 of SuperI/O Configuration 1 register (index 21h).

2.2 SOFTWARE CONFIGURATION

2.2.1 Accessing the Configuration Registers

Only two system I/O addresses are required to access any of the configuration registers. The Index and Data register pair is used to access registers for all read and write operations.

In a write operation, the target configuration register is identified, based on a value that is loaded into the Index register. Then, the data to be written into the configuration register is transferred via the Data register.

Similarly, for a read operation, first the source configuration register is identified, based on a value that is loaded into the Index register. Then, the data to be read is transferred via the Data register.

Reading the Index register returns the last value loaded into the Index register. Reading the Data register returns the data in the configuration register pointed to by the Index register.

If, during reset, the Base Address 1 (BADDR1) signal is low (0), the Index and Data registers are not accessible immediately after reset. As a result, all configuration registers of the PC87308VUL are also not accessible at this time. To access these registers, you must apply the Plug and Play (PnP) ISA protocol.

If during reset, the Base Address 1 (BADDR1) signal is high (1), all configuration registers are accessible immediately after reset.

It is up to the configuration software to guarantee no conflicts between the registers of the active (enabled) logical devices, between IRQ signals and between DMA channels. If conflicts of this type occur, the results are unpredictable.

2.2.2 Address Decoding

In full Plug and Play mode, the addresses of the Index and Data registers that access the configuration registers are decoded using pins A11-0, according to the ISA Plug and Play specification.

In Plug and Play Motherboard mode, the addresses of the Index and Data registers that access the configuration registers are decoded using pins A15-1. Pin A0 distinguishes between these two registers.

KBC and mouse register addresses are decoded using pins A1,0 and A15-3. Pin A2 distinguishes between the device registers.

RTC/APC and Power Management (PM) register addresses are decoded using pins A15-1. PM has only five registers and only responds to accesses to those registers.

FDC, UART, and GPIO register addresses are decoded using pins A15-3 pins.

Parallel Port (PP) modes determine which pins are used tor register addresses. In SPP mode, 14 pins are used to decode Parallel Port (PP) base addresses. In ECP and EPP modes, 13 address pins are used. Table 2-3 shows which address pins are used in each mode.

TABLE 2-3. Address Pins Used for Parallel Port

PP Mode	Pins Used to Decode Base Address	Pins Used to Distinguish Registers
SPP	A15-2	A1,0
ECP	A9-2 and A15-11	A1,0 and A10
EPP	A15-3	A2-0

TABLE 2-4. Parallel Port Address Range Allocation

Parallel Port Mode	SuperI/O Parallel Port Configuration Register Bits 7 6 5 4	Decoded Range [a]
SPP	0 0 x x	Three registers, from base to base + 02h
EPP (Non ECP Mode 4)	0 1 x x	Eight registers, from base to base + 07h
ECP, No Mode 4, No Internal Configuration	1 0 0 0	Six registers, from base to base + 02h and from base + 400h to base + 402h
ECP with Mode 4, No Internal Configuration	1 1 1 0	11 registers, from base to base + 07h and from base + 400h to base + 402h
ECP with Mode 4, Configuration within Parallel Port	1 0 0 1 or 1 1 1 1	16 registers, from base to base + 07h and from base + 400h to base + 407h

a. The SuperI/O processor does not decode the Parallel Port outside this range.

2.3 THE CONFIGURATION REGISTERS

The configuration registers control the setup of the PC87308VUL. Their major functions are to:

- Identify the chip
- Enable major functions (such as, the Keyboard Controller (KBC) for the keyboard and the mouse, the Real-Time Clock (RTC), including Advanced Power Control (APC), the Floppy Disc Controller (FDC), UARTs, parallel and general purpose ports, power management and pin functionality)
- Define the I/O addresses of these functions
- Define the status of these functions upon reset

Section 2.3.2 summarizes information for each register of each function. In addition, the following non-standard, or card control, registers are described in detail, in Section 2.4 starting on page 21.

- Card Control Registers
  - — SuperI/O Configuration 1 Register
  - — SuperI/O Configuration 2 Register
  - — Programmable Chip Select Configuration Index Register
  - — Programmable Chip Select Configuration Data Register
- KBC Configuration Register (Logical Device 0)
  - — SuperI/O KBC Configuration Register
- FDC Configuration Registers (Logical Device 3)
  - — SuperI/O FDC Configuration Register
  - — Drive ID Register
- Parallel Port Configuration Register (Logical Device 4)
  - — SuperI/O Parallel Port Configuration Register
- UART2 and Infrared Configuration Register (Logical Device 5)
  - — SuperI/O UART2 Configuration Register
- UART1 Configuration Register (Logical Device 6)
  - — SuperI/O UART1 Configuration Register
- Programmable Chip Select Configuration Registers
  - — $\overline{CS0}$ Base Address MSB Register
  - — $\overline{CS0}$ Base Address LSB Register
  - — $\overline{CS0}$ Configuration Register
  - — $\overline{CS1}$ Base Address MSB Register
  - — $\overline{CS1}$ Base Address LSB Register
  - — $\overline{CS1}$ Configuration Register
  - — $\overline{CS2}$ Base Address MSB Register
  - — $\overline{CS2}$ Base Address LSB Register
  - — $\overline{CS2}$ Configuration Register

2.3.1 Standard Plug and Play (PnP) Register Definitions

Tables 2-5 through 2-10 describe the standard Plug and Play registers. For more detailed information on these registers, refer the *"Plug and Play ISA Specification, Version 1.0a, May 5, 1994."*.

TABLE 2-5. Plug and Play (PnP) Standard Control Registers

Index	Name	Definition
00h	Set RD_DATA Port	Writing to this location modifies the address of the port used for reading from the Plug and Play ISA cards. Data bits 7-0 are loaded into I/O read port address bits 9-2. Reads from this register are ignored. Bits1 and 0 are fixed at the value 11.
01h	Serial Isolation	Reading this register causes a Plug and Play card in the Isolation state to compare one bit of the ID of the board. This register is read only.
02h	Config Control	This register is write-only. The values are not sticky, that is, hardware automatically clears the bits and there is no need for software to do so. Bit 0 - Reset Writing this bit resets all logical devices and restores the contents of configuration registers to their power-up (default) values. In addition, all the logical devices of the card enter their default state and the CSN is preserved. Bit 1 - Return to the Wait for Key state. Writing this bit puts all cards in the Wait for Key state, with all CSNs preserved and logical devices not affected. Bit 2 - Reset CSN to 0. Writing this bit causes every card to reset its CSN to zero.
03h	Wake[CSN]	A write to this port causes all cards that have a CSN that matches the write data in bits 7-0 to go from the Sleep state to either the Isolation state, if the write data for this command is zero, or the Config state, if the write data is not zero. It also resets the pointer to the byte-serial device. This register is write-only.
04h	Resource Data	This address holds the next byte of resource information. The Status register must be polled until bit 0 of this register is set to 1 before this register can be read. This register is read-only.
005	Status	When bit 0 of this register is set to 1, the next data byte is available for reading from the Resource Data register. This register is read-only.
06h	Card Select Number (CSN)	Writing to this port assigns a CSN to a card. The CSN is a value uniquely assigned to each ISA card after the serial identification process so that each card may be individually selected during a Wake[CSN] command. This register is read/write.
07h	Logical Device Number	This register selects the current logical device. All reads and writes of memory, I/O, interrupt and DMA configuration information access the registers of the logical device written here. In addition, the I/O Range Check and Activate commands operate only on the selected logical device. This register is read/write. If a card has only 1 logical device, this location should be a read-only value of 00h.
20h - 2Fh	Card Level, Vendor Defined	Vendor defined registers.

TABLE 2-6. Plug and Play (PnP) Logical Device Control Registers

Index	Name	Definition
0030h	Activate	For each logical device there is one Activate register that controls whether or not the logical device is active on the ISA bus. This is a read/write register. Before a logical device is activated, I/O Range Check must be disabled. Bit 0 - Logical Device Activation Control 0 - Do not activate the logical device. 1 - Activate the logical device. Bits 7-1 - Reserved These bits are reserved and must return 0 on reads.
0031h	I/O Range Check	This register is used to perform a conflict check on the I/O port range programmed for use by a logical device. This register is read/write. Bit 0 - I/O Range Check control 0 - The logical device drives 00AAh. 1 - The logical device responds to I/O reads of the logical device's assigned I/O range with a 0055h when I/O Range Check is enabled. Bit 1 - Enable I/O Range Check 0 - I/O Range Check is disabled. 1 - I/O Range Check is enabled. (I/O Range Check is valid only when the logical device is inactive). Bits 7-2 - Reserved These bits are reserved and must return 0 on reads.

TABLE 2-7. Plug and Play (PnP) I/O Space Configuration Registers

Index	Name	Definition
60h	I/O Port Base Address Bits (15-8) Descriptor 0	Read/write value indicating the selected I/O lower limit address bits 15-8 for I/O descriptor 0.
61h	I/O Port Base Address Bits (7-0) Descriptor 0	Read/write value indicating the selected I/O lower limit address bits 7-0 for I/O descriptor 0.
62h	I/O Port Base Address Bits (15-8) Descriptor 1	Read/write value indicating the selected I/O lower limit address bits 15-8 for I/O descriptor 1.
63h	I/O Port Base Address Bits (7-0) Descriptor 1	Read/write value indicating the selected I/O lower limit address bits 7-0 for I/O descriptor 1.

TABLE 2-8. Plug and Play (PnP) Interrupt Configuration Registers

Index	Name	Definition
70h	Interrupt Request Level Select 0	Read/write value indicating selected interrupt level. Bits3-0 select the interrupt level used for interrupt 0. A value of 1 selects IRQL 1, a value of 15 selects IRQL 15. IRQL 0 is not a valid interrupt selection and (represents no interrupt selection.
71h	Interrupt Request Type Select 0	Read/write value that indicates the type and level of the interrupt request level selected in the previous register. If a card supports only one type of interrupt, this register may be read-only. Bit 0 - Type of the interrupt request selected in the previous register. 0 - Edge 1 - Level Bit1 - Level of the interrupt request selected in the previous register. (See also “IRQ Mapping” on page 164). 0 - Low polarity (implies open-drain output with strong pull-up for a short time, followed by weak pull-up). 1 - High polarity (implies push-pull output).

TABLE 2-9. Plug and Play (PnP) DMA Configuration Registers

Index	Name	Definition
74h	DMA Channel Select 0	Read/write value indicating selected DMA channel for DMA 0. Bits 2-0 select the DMA channel for DMA 0. A value of 0 selects DMA channel 0; a value of 7 selects DMA channel 7. Selecting DMA channel 4, the cascade channel, indicates that no DMA channel is active.
75h	DMA Channel Select 1	Read/write value indicating selected DMA channel for DMA 1 Bits 2-0 select the DMA channel for DMA 1. A value of 0 selects DMA channel 0; a value of 7 selects DMA channel 7. Selecting DMA channel 4, the cascade channel, indicates that no DMA channel is active.

TABLE 2-10. Plug and Play (PnP) Logical Device Configuration Registers

Index	Name	Definition
F0h-FEh	Logical Device Configuration Vendor Defined	Vendor defined.

2.3.2 Configuration Register Summary

The tables in this section specify the Index, type (read/write), reset value and configuration register or action that controls each register associated with each function. When the reset value is not fixed, the table indicates what controls the value or points to another section that provides this information.

Soft Reset indicates a Reset executed by using the Reset Bit (Bit 0) of the Config Control Register. (See Table 2-5 on page 14.)

TABLE 2-11. Card Configuration Registers

Index	Type	Hard Reset	Soft Reset	Configuration Register or Action
00h	W	00h	PnP ISA	Set RD_DATA Port.
01h	R			Serial Isolation.
02h	W	PnP ISA	PnP ISA	Configuration Control.
03h	W	00h	PnP ISA	Wake[CSN].
04h	R			Resource Data.
05h	R			Status.
06h	R/W	00h	PnP ISA	Card Select Number (CSN).
07h	R/W	00h	PnP ISA	Logical Device Number.
20h	R	A0h	A0h	SID Register. Bits 2-0 - Revision ID Bit 7-3 - Chip ID
21h	R/W	See Section 2.4.1 on page 21.	No Effect	SuperI/O Configuration 1 Register.
22h	R/W	See Section 2.4.2 on page 22.	No Effect	SuperI/O Configuration 2 Register.
23h	R/W	See Section 2.4.3 on page 22.	No Effect	Programmable Chip Select Configuration Index Register.
24h	R/W	See Section 2.4.4 on page 22.	No Effect	Programmable Chip Select Configuration Data Register.

TABLE 2-12. KBC Configuration Registers for Keyboard - Logical Device 0

Index	R/W	Hard Reset	Soft Reset	Configuration Register or Action
30h	R/W	00h or 01h See CFG0 in Section 2.1.3.	00h or 01h See CFG0 in Section 2.1.3.	Activate. See also FER1 of power management device (logical device 8).
31h	R/W	00h	00h	I/O Range Check.
60h	R/W	00h	00h	Data Base Address MSB Register.
61h	R/W	60h	60h	Data Base Address LSB Register. Bit 2 (for A2) is read only, 0.
62h	R/W	00h	00h	Command Base Address MSB Register.
63h	R/W	00h	00h	Command Base Address LSB. Bit 2 (for A2) is read only,1.
70h	R/W	01h	01h	KBD Interrupt (KBC IRQ1 pin) Select.
71h	RW	02h	02h	KBD Interrupt Type. Bits 1,0 are read/write; other bits are read only.
74h	R	04h	04h	Report no DMA assignment.
75h	R	04h	04h	Report no DMA assignment.
F0h	R/W	See Section 2.5.1 on page 23.	No Effect	SuperI/O KBC Configuration Register.

TABLE 2-13. KBC Configuration Registers for Mouse - Logical Device 1

Index	R/W	Hard Reset	Soft Reset	Configuration Register or Action
30h	R/W	00h	00h	Activate. When mouse of the KBC mouse is inactive, the IRQ selected by the Mouse Interrupt Select register (index 70h) is not asserted. This register has no effect on host KBC commands handling the PS/2 mouse.
70h	R/W	0Ch	0Ch	Mouse Interrupt (KBC IRQ12 pin) Select.
71h	R/W	02h	02h	Mouse Interrupt Type. Bits 1,0 are read/write; other bits are read only.
74h	R	04h	04h	Report no DMA assignment.
75h	R	04h	04h	Report no DMA assignment.

TABLE 2-14. RTC and APC Configuration Registers - Logical Device 2

Index	R/W	Hard Reset	Soft Reset	Configuration Register or Action
30h	R/W	00h or 01h See CFG0 in Section 2.1.3.	00h or 01h See CFG0 in Section 2.1.3.	Activate. The APC of the RTC is not affected by bit 0. See also FER1 of logical device 8.
31h	R/W	00h	00h	I/O Range Check.
60h	R/W	00h	00h	Base Address MSB Register.
61h	R/W	70h	70h	Base Address LSB Register. Bit 0 (for A0) is read only, 0.
70h	R/W	08h	08h	Interrupt Select.
71h	R/W	00h	00h	Interrupt Type. Bit 1 is read/write, other bits are read only.
74h	R	04h	04h	Report no DMA assignment.
75h	R	04h	04h	Report no DMA assignment.

TABLE 2-15. FDC Configuration Registers - Logical Device 3

Index	R/W	Hard Reset	Soft Reset	Configuration Register or Action
30h	R/W	00h or 01h See CFG0 in Section 2.1.3.	00h or 01h See CFG0 in Section 2.1.3.	Activate. See also FER1 of logical device 8.
31h	R/W	00h	00h	I/O Range Check.
60h	R/W	03h	03h	Base Address MSB Register.
61h	R/W	F0h	F0h	Base Address LSB Register. Bits 2-0 (for A2-0) are read only, 000.
70h	R/W	06h	06h	Interrupt Select.
71h	R/W	03h	03h	Interrupt Type. Bit 1 is read/write; other bits are read only.
74h	R/W	02h	02h	DMA Channel Select.
75h	R	04h	04h	Report no DMA assignment.
F0h	R/W	See Section 2.6.1 on page 23.	No Effect	SuperI/O FDC Configuration Register.
F1h	R/W	See Section 2.6.2 on page 23.	No Effect	Drive ID Register.

TABLE 2-16. Parallel Port Configuration Registers - Logical Device 4

Index	R/W	Hard Reset	Soft Reset	Configuration Register or Action
30h	R/W	00h	00h	Activate. See also FER1 of the power management device (logical device 8).
31h	R/W	00h	00h	I/O Range Check.
60h	R/W	02h	02h	Base Address MSB register. Bits 7-2 (for A15-10) are read only, 000000.
61h	R/W	78h	78h	Base Address LSB register. Bits 1,0 (for A1,0) are read only, 00. See Section 2.2.2 on page 12.
70h	R/W	07h	07h	Interrupt Select.
71h	R/W	00h	00h	Interrupt Type. Bit 0 is read only. It reflects the interrupt type dictated by the Parallel Port operation mode and configured by the SuperI/O Parallel Port Configuration register. This bit is set to 1 (level interrupt) in Extended Mode and cleared (edge interrupt) in all other modes. Bit 1 is a read/write bit. Bits 7-2 are read only.
74h	R/W	04h	04h	DMA Channel Select.
75h	R	04h	04h	Report no DMA assignment.
F0h	R/W	See Section 2.7 on page 24	No Effect	SuperI/O Parallel Port Configuration register.

TABLE 2-17. UART2 and Infrared Configuration Registers - Logical Device 5

Index	R/W	Hard Reset	Soft Reset	Configuration Register or Action
30h	R/W	00h	00	Activate. See also FER1 of the power management device (logical device 8).
31h	R/W	00h	00h	I/O Range Check.
60h	R/W	02h	02h	Base Address MSB register.
61h	R/W	F8h	F8h	Base Address LSB register. Bit 2-0 (for A2-0) are read only, 000.
70h	R/W	03h	03h	Interrupt Select.
71h	R/W	03h	03h	Interrupt Type. Bit 1 is R/W; other bits are read only.
74h	R/W	04h	04h	DMA Channel Select 0 (RX_DMA).
75h	R/W	04h	04h	DMA Channel Select 1 (TX_DMA).
F0h	R/W	See Section 2.8 on page 24	No Effect	SuperI/O UART 2 Configuration register.

TABLE 2-18. UART1 Configuration Registers - Logical Device 6

Index	R/W	Hard Reset	Soft Reset	Configuration Register or Action
30h	R/W	00h	00h	Activate. See also FER1 of the power management device (logical device 8).
31h	R/W	00h	00h	I/O Range Check.
60h	R/W	03h	03h	Base Address MSB Register.
61h	R/W	F8h	F8h	Base Address LSB Register. Bits 2-0 (for A2-0) are read only as 000.
70h	R/W	04h	04h	Interrupt Select.
71h	R/W	03h	03h	Interrupt Type. Bit 1 is read/write. Other bits are read only.
74h	R	04h	04h	Report no DMA Assignment.
75h	R	04h	04h	Report no DMA Assignment.
F0h	R/W	See Section 2.9.1 on page 25	No Effect	SuperI/O UART 1 Configuration register.

TABLE 2-19. GPIO Ports Configuration Registers - Logical Device 7

Index	R/W	Hard Reset	Soft Reset	Configuration Register or Action
30h	R/W	00h	00h	Activate. See also FER2 of the power management device (logical device 8).
31h	R/W	00h	00h	I/O Range Check.
60h	R/W	00h	00h	Base Address MSB Register.
61h	R/W	00h	00h	Base Address LSB Register. Bit 3-0 (for A3-0) are read only: 0000.
74h	R	04h	04h	Report no DMA assignment.
75h	R	04h	04h	Report no DMA assignment.

TABLE 2-20. Power Management Configuration Registers - Logical Device 8

Index	R/W	Hard Reset	Soft Reset	Configuration Register or Action
30h	R/W	00	00	Activate. When bit 0 is cleared, the registers of this logical device are not accessible. The registers are maintained.
31h	R/W	00h	00h	I/O Range Check.
60h	R/W	00h	00h	Base Address Most Significant Byte.
61h	R/W	00h	00h	Base Address LSB Register. Bit 0 (for A) is read only: 0.
74h	R	04h	04h	Report no DMA assignment.
75h	R	04h	04h	Report no DMA assignment.

2.4 CARD CONTROL REGISTERS

This section describes the registers at first level indexes in the range 20h - 2Fh.

The next section describes the chip select configuration registers, which are accessed using two index levels. The first index level accesses the Programmable Chip Select Index register at 23h. The second index level accesses a specific chip select configuration register. See Table 2-22 on page 25.

2.4.1 SuperI/O Configuration 1 Register, Index 21h

This register can be read or written. It is reset by hardware to 04h, 06h, 14h or 16h. See SELCS and the CFG1 strap pin in Table 2-2 on page 12.

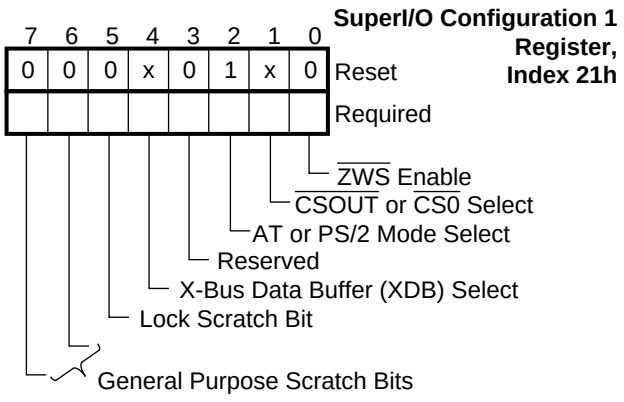


FIGURE 2-1. SuperI/O Configuration 1 Register Bitmap

Bit 0 - $\overline{\text{ZWS}}$ Enable

This bit controls assertion of $\overline{\text{ZWS}}$ on any host SuperI/O chip access, except for configuration registers access (including Serial Isolation register) and except for Parallel Port access.

For $\overline{\text{ZWS}}$ assertion on host-EPP access, see Section 6.5.17 on page 99.

0 - $\overline{\text{ZWS}}$ is not asserted.

1 - $\overline{\text{ZWS}}$ is asserted.

Bit 1 - $\overline{\text{CSOUT}}$-NSC-test or $\overline{\text{CS0}}$ Pin Select

This bit is initialized with SELCS strap value.

0 - $\overline{\text{CSOUT}}$-NSC-test on $\overline{\text{CS0}}$ pin.

1 - $\overline{\text{CS0}}$.

Bit 2 - PC-AT or PS/2 Drive Mode Select

0 - PS/2 mode.

1 - PC-AT mode. (Default)

Bit 3 - Reserved

Reserved.

Bit 4 - X-Bus Data Buffer (XDB) Select

Select X-bus buffer on the XDB pins. This read only bit is initialized with the CFG1 strap value. See also Chapter 10 on page 162.

0 - No XDB buffer. XDB pins have alternate function, see Table 1-2 on page 10.

1 - XDB enabled.

Bit 5 - Lock Scratch Bit

This bit controls bits 7 and 6 of this register. Once this bit is set to 1 by software, it can be cleared to 0 only by a hardware reset.

0 - Bits 7 and 6 of this register are read/write bits.

1 - Bits 7 and 6 of this register are read only bits.

Bits 7,6 - General Purpose Scratch Bits

When bit 5 is set to 1, these bits are read only. After reset they can be read or written. Once changed to read-only, they can be changed back to be read/write bits only by a hardware reset.

2.4.2 SuperI/O Configuration 2 Register, Index 22h

This read/write register is reset by hardware to 00h-03h. See BADDR1,0 strap pins in Section 2.1.3.

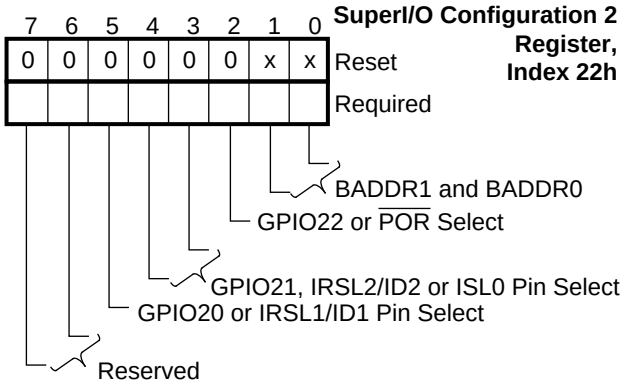


FIGURE 2-2. SuperI/O Configuration 2 Register Bitmap

Bits 1,0 - BADDR1 and BADDR0

Initialized on reset by BADDR1 and BADDR0 strap pins (BADDR0 on bit 0). These bits select the addresses of the configuration Index and Data registers and the Plug and Play ISA Serial Identifier. See Tables 2-1 and 2-2.

Bit 2 - GPIO22 or $\overline{\text{POR}}$ Pin Select

The output buffer of this pin is selected by Port 2 Output Type and Port 2 Pull-up Control registers.

0 - The pin is GPIO22.

1 - The pin is $\overline{\text{POR}}$.

Bits 4,3 - GPIO21, IRSL2/ID2 or IRSL0 Pin Select

The output buffer of this pin is selected by Port 2 Output Type and Port 2 Pull-up Control registers as shown in Table 2-21.

TABLE 2-21. Signal Assignment for Pins 158 and 77

Bit 4 3	Pin 158	Pin 77 when Bit 4 of SuperI/O Config 1 Register = 0
0 0	GPIO21	IRSL2/SELCS
0 1	IRSL2/ID2	GPIO21/SELCS
1 0	IRSL0	IRSL2/SELCS
1 1	Reserved	IRSL2/SELCS

Bit 5 - GPIO20, IRSL1/ID1 Pin Select

The output buffer of this pin is selected by Port 2 Output Type and Port 2 Pull-up Control registers.

0 - The pin is GPIO20.

1 - The pin is IRSL1/ID1.

Bits 7,6 - Reserved

Reserved. Return 0 when read.

2.4.3 Programmable Chip Select Configuration Index Register, Index 23h

This read/write register is reset by hardware to 00h. It indicates the index of one of the Programmable Chip Select ($\overline{\text{CS0}}$, $\overline{\text{CS1}}$ or $\overline{\text{CS2}}$) configuration registers described in Section 2.10.

The data in the indicated register is in the Programmable Chip Select Configuration Data register at index 24h.

Bits 7 through 4 are read only and return 0000 when read.

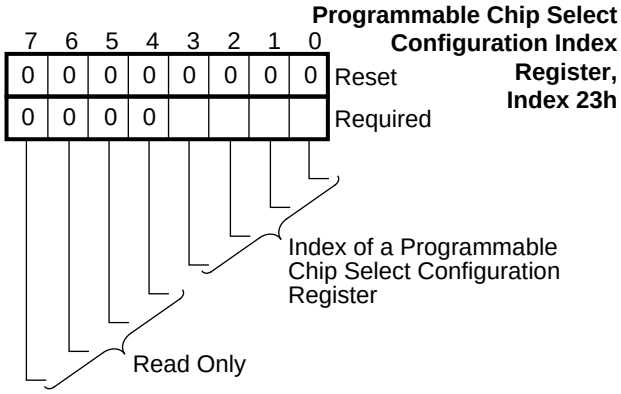


FIGURE 2-3. Programmable Chip Select Configuration Index Register Bitmap

2.4.4 Programmable Chip Select Configuration Data Register, Index 24h

This read/write register contains the data in the Programmable Chip Select Configuration register (see Section 2.10) indicated by the Programmable Chip Select Configuration Index register at index 23h.

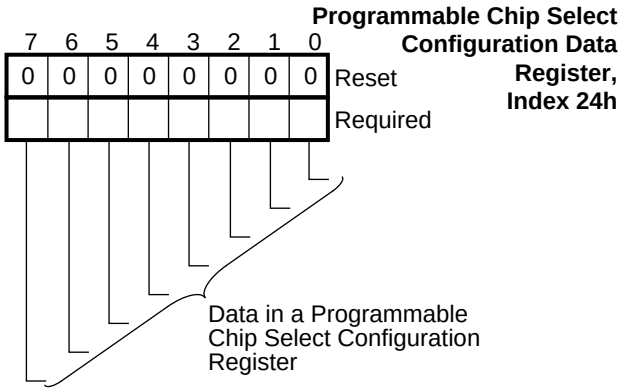


FIGURE 2-4. Programmable Chip Select Configuration Data Register Bitmap

2.5 KBC CONFIGURATION REGISTER (LOGICAL DEVICE 0)

2.5.1 SuperI/O KBC Configuration Register, Index F0h

This read/write register is reset by hardware to 40h.

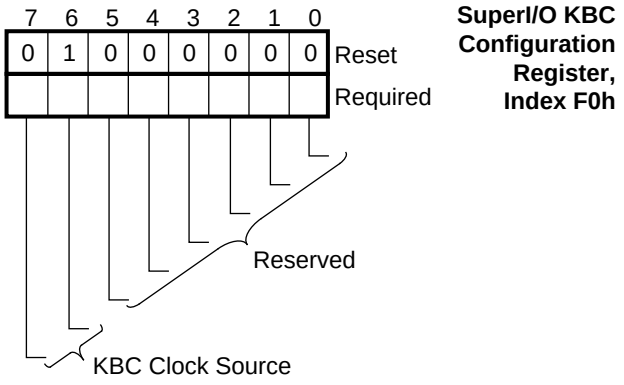


FIGURE 2-5. SuperI/O KBC Configuration Register Bitmap

Bits 5-0 - Reserved

Reserved.

Bits 7,6 - KBC Clock Source

Bit 6 is the LSB. The clock source can be changed only when the KBC is inactive (disabled).

00 - 8 MHz

01 - 12 MHz

10 - 16 MHz. Undefined results when these bits are 10 and the clock source for the chip is 24 MHz on X1.

11 - Reserved.

2.6 FDC CONFIGURATION REGISTERS (LOGICAL DEVICE 3)

2.6.1 SuperI/O FDC Configuration Register, Index F0h

This read/write register is reset by hardware to 20h.

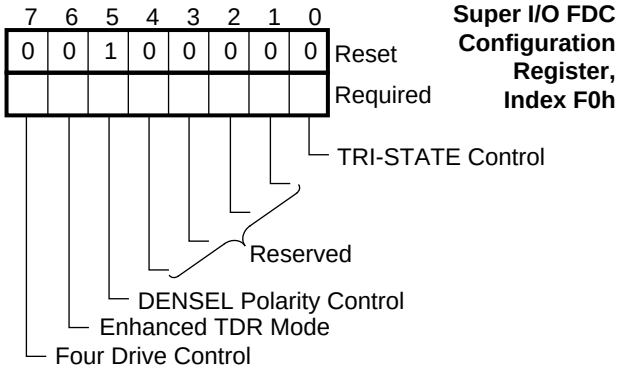


FIGURE 2-6. SuperI/O FDC Configuration Register Bitmap

Bit 0 - TRI-STATE Control

When set, this bit causes the FDC pins to be in TRI-STATE (except the IRQ and DMA pins) when the FDC is inactive (disabled).

This bit is ORed with a bit of PMC1 register of logical device 8.

0 - FDC pins are not put in TRI-STATE.

1 - FDC pins are put in TRI-STATE.

Bits 4-1 - Reserved

Reserved.

Bit 5 - DENSEL Polarity Control

0 - DENSEL is active low for 500 Kbps or 1 Mbps data rates.

1 - DENSEL is active high for 500 Kbps or 1 Mbps data rates. (Default)

Bit 6 - Enhanced TDR Mode

0 - AT Compatible TDR Mode (bits 7 through 2 of TDR not driven).

1 - Enhanced TDR Mode (bits 7 through 2 of TDR driven on TDR read).

Bit 7 - Four Drive Encode

0 - Two floppy drives are directly controlled by $\overline{\text{DR1-0}}$, $\overline{\text{MTR1-0}}$.

1 - Four floppy drives are controlled with the aid of an external decoder.

2.6.2 Drive ID Register, Index F1h

This read/write register is reset by hardware to 00h. These bits control bits 5 and 4 of the enhanced TDR register.

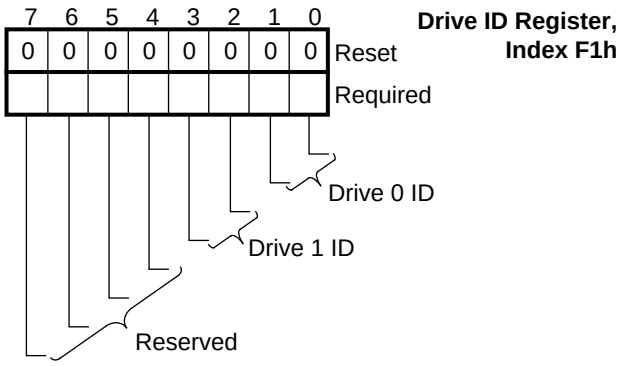


FIGURE 2-7. Drive ID Register Bitmap

Bits 1,0 - Drive 0 ID

These bits are reflected on bits 5 and 4, respectively, of the Tape Drive Register (TDR) of the FDC when drive 0 is accessed. See Section 5.2.4 on page 61.

Bits 3,2 - Drive 1 ID

These bits are reflected on bits 5 and 4, respectively, of the TDR register of the FDC when drive 1 is accessed. See Section 5.2.4 on page 61.

Bits 7-4 - Reserved

These bits are reserved.

2.7 PARALLEL PORT CONFIGURATION REGISTER (LOGICAL DEVICE 4)

2.7.1 SuperI/O Parallel Port Configuration Register, Index F0h

This read/write register is reset by hardware to F2h. For normal operation and to maintain compatibility with future chips, do not change bits 7 through 4.

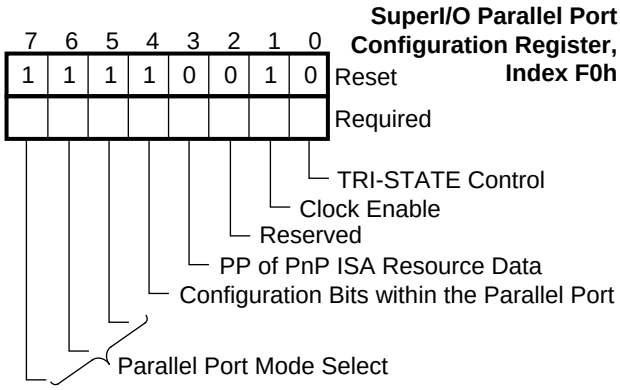


FIGURE 2-8. SuperI/O Parallel Port Configuration Register Bitmap

Bit 0 - TRI-STATE Control

When set, this bit causes the parallel port pins to be in TRI-STATE (except IRQ and DMA pins) when the parallel port is inactive (disabled). This bit is ORed with a bit of the PMC1 register of logical device 8.

Bit 1 - Clock Enable

0 - Parallel port clock disabled.

ECP modes and EPP time-out are not functional when the logical device is active. Registers are maintained.

1 - Parallel port clock enabled.

All operation modes are functional when the logical device is active. This bit is ANDed with a bit of the PMC3 register of the power management device (logical device 8).

Bit 2 - Reserved

This bit is reserved.

Bit 3 - Reported Parallel Port of PnP ISA Resource Data

Report to the ISA PnP Resource Data the device identification.

0 - ECP device.

1 - SPP device.

Bit 4 - Configuration Bits within the Parallel Port

0 - The registers at base (address) + 403h, base + 404h and base + 405h are not accessible (reads and writes are ignored).

1 - When ECP is selected by bits 7 through 5, the registers at base (address) + 403h, base + 404h and base + 405h are accessible.

This option supports run-time configuration within the Parallel Port address space. An 8-byte (and 1024-byte) aligned base address is required to access these registers. See Chapter 6 on page 84 for details.

Bit 7-5 - Parallel Port Mode Select

Bit 5 is the LSB.

Selection of EPP 1.7 or 1.9 in ECP mode 4 is controlled by bit 4 of the Control2 configuration register of the parallel port at offset 02h. See Section 6.5.17 on page 99.

000 - SPP Compatible mode. PD7-0 are always output signals.

001 - SPP Extended mode. PD7-0 direction controlled by software.

010 - EPP 1.7 mode.

011 - EPP 1.9 mode.

100 - ECP mode (IEEE1284 register set), with no support for EPP mode .

101 - Reserved.

110 - Reserved.

111 - ECP mode (IEEE1284 register set), with EPP mode selectable as mode 4.

2.8 UART2 AND INFRARED CONFIGURATION REGISTER (LOGICAL DEVICE 5)

2.8.1 SuperI/O UART2 Configuration Register, Index F0h

This read/write register is reset by hardware to 02h.

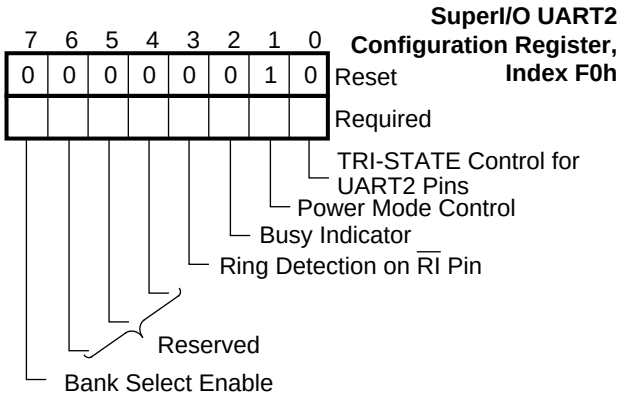


FIGURE 2-9. SuperI/O UART2 Configuration Register Bitmap

Bit 0 - TRI-STATE Control for UART Pins

This bit controls the TRI-STATE status of UART signals (except IRQ and DMA pins) when the UART is inactive (disabled). This bit is ORed with a bit of the PMC1 register of the power management device (logical device 8).

0 - Pins not in TRI-STATE.

1- Pins in TRI-STATE.

Bit 1 - Power Mode Control

0 - Low power mode.

UART Clock disabled. UART output signals are set to their default state. The $\overline{RI}$ input signal can be programmed to generate an interrupt. Registers are maintained.

1 - Normal power mode.

UART clock enabled. The UART is functional when the logical device is active. This bit is ANDed with a bit of the PMC3 register of the power management device (logical device 8).

Bit 2 - Busy Indicator

This read-only bit can be used by power management software to decide when to power down the logical device. This bit is also accessed via the PMC3 register of the power management device (logical device 8).

0 - No transfer in progress.

1 - Transfer in progress.

Bit 3 - Ring Detection on $\overline{RI}$ Pin

0 - The UART $\overline{RI}$ input signal uses the $\overline{RI}$ pin.

1 - The UART $\overline{RI}$ input signal is the $\overline{RING}$ detection signal on the $\overline{RING}$ pin. $\overline{RING}$ pin is selected by the APCR2 register of the APC.

Bits 6-4 - Reserved

These bits are reserved.

Bit 7 - Bank Select Enable

Enables bank switching. If this bit is cleared, all attempts to access the extended registers are ignored.

2.9 UART1 CONFIGURATION REGISTER (LOGICAL DEVICE 6)

2.9.1 SuperI/O UART1 Configuration Register, Index F0h

This read/write register is reset by hardware to 02h. Same as the SuperI/O UART2 Configuration register, except for bit 2. Bit 2 is reserved and returns 0 when read .

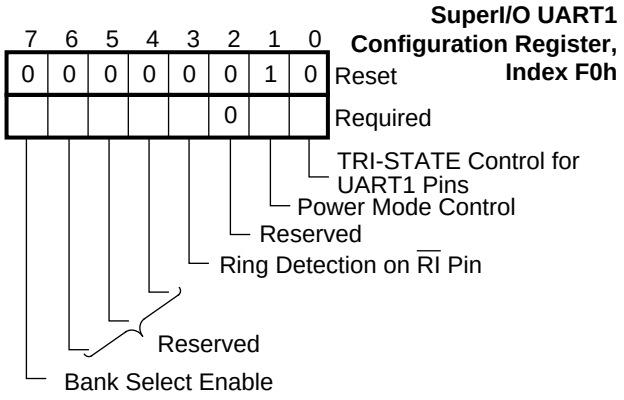


FIGURE 2-10. SuperI/O UART1 Configuration Register Bitmap

2.10 PROGRAMMABLE CHIP SELECT CONFIGURATION REGISTERS

The chip select configuration registers are accessed using two index levels. The first index level accesses the Programmable Chip Select Index register at 23h. See Section 2.4.3 on page 22. The second index level accesses a specific chip select configuration register as shown in Table 2-22.

TABLE 2-22. The Programmable Chip Select Configuration Registers

Second Level Index	Register Name	Type	Reset
00h	$\overline{CS0}$ Base Address MSB Register	R/W	00h
01h	$\overline{CS0}$ Base Address LSB Register	R/W	00h
02h	$\overline{CS0}$ Configuration Register	R/W	00h
03h	Reserved	-	-
04h	$\overline{CS1}$ Base Address MSB Register	R/W	00h
05h	$\overline{CS1}$ Base Address LSB Register	R/W	00h
06h	$\overline{CS1}$ Configuration Register	R/W	00h
07h	Reserved	-	-
08h	$\overline{CS2}$ Base Address MSB Register	R/W	00h
09h	$\overline{CS2}$ Base Address LSB Register	R/W	00h
0Ah	$\overline{CS2}$ Configuration Register	R/W	00h
0Bh-0Fh	Reserved	-	-
10h-FFh	Not Accessible	-	-

See also, “Programmable Chip Select Output Signals” on page 157 and the description of each signal in Table 1-1 on page 2.

2.10.1 $\overline{CS0}$ Base Address MSB, Second Level Index 00h

This read/write register is reset by hardware to 00h. Same as Plug and Play ISA base address register at index 60h. See Table 2-7 on page 15.

2.10.2 $\overline{CS0}$ Base Address LSB Register, Second Level Index 01h

This read/write register is reset by hardware to 00h. It is the same as the Plug and Play ISA base address register at index 61h. See Table 2-7 on page 15.

2.10.3 $\overline{CS0}$ Configuration Register, Second Level Index 02h

This read/write register is reset by hardware to 00h. This register controls activation of the $\overline{CS0}$ signal upon an address match, when AEN is inactive (low) and the non-masked address pins match the corresponding base address bits.

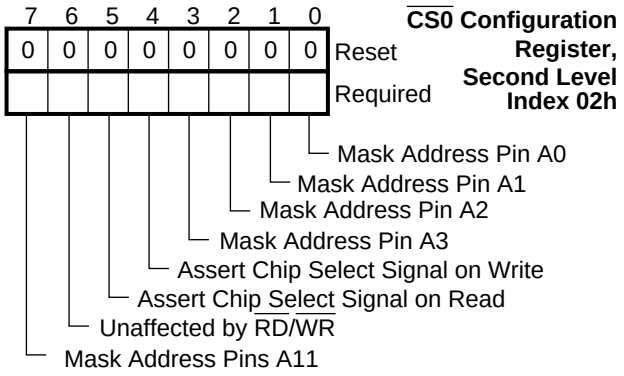


FIGURE 2-11. $\overline{CS0}$ Configuration Register Bitmap

Bit 0 - Mask Address Pin A0

0 - A0 is decoded.

1 - A0 is not decoded; it is ignored.

Bit 1 - Mask Address Pin A1

0 - A1 is decoded.

1 - A1 is not decoded (ignored).

Bit 2 - Mask Address Pin A2

0 - A2 is decoded.

1 - A2 is not decoded; it is ignored.

Bit 3 - Mask Address Pin A3

0 - A3 is decoded.

1 - A3 is not decoded; it is ignored.

Bit 4 - Assert Chip Select Signal on Write

0 - Chip select not asserted on address match and when $\overline{WR}$ is active (low).

1 - Chip select asserted on address match and when $\overline{WR}$ is active (low).

Bit 5 - Assert Chip Select Signal on Read

0 - Chip select not asserted on address match and when $\overline{RD}$ is active (low).

1 - Chip select asserted on address match and when $\overline{RD}$ is active (low).

Bit 6 - Unaffected by $\overline{RD}$ 0r $\overline{WR}$

Bits 5 and 4 are ignored when this bit is set.

0 - Chip select asserted on address match, qualified by $\overline{RD}$ or $\overline{WR}$ pin state and contents of bits 5 and 4.

1 - Chip select asserted on address match, regardless of $\overline{RD}$ or $\overline{WR}$ pin state and regardless of contents of bits 5 and 4.

Bit 7 - Mask Address Pins A11-A0

0 - A11 are decoded.

1 - A11 are not decoded; they are ignored.

2.10.4 Reserved, Second Level Index 03h

Attempts to access this register produce undefined results.

2.10.5 $\overline{CS1}$ Base Address MSB Register, Second Level Index 04h

This read/write register is reset by hardware to 00h. Same as Plug and Play ISA base address register at index 60h. See Table 2-7 on page 15.

2.10.6 $\overline{CS1}$ Base Address LSB Register, Second Level Index 05h

This read/write register is reset by hardware to 00h. Same as Plug and Play ISA base address register at index 61h. See Table 2-7 on page 15.

2.10.7 $\overline{CS1}$ Configuration Register, Second Level Index 06h

This read/write register is reset by hardware to 00h. Same as $\overline{CS0}$ Configuration Register described in Section 2.10.3.

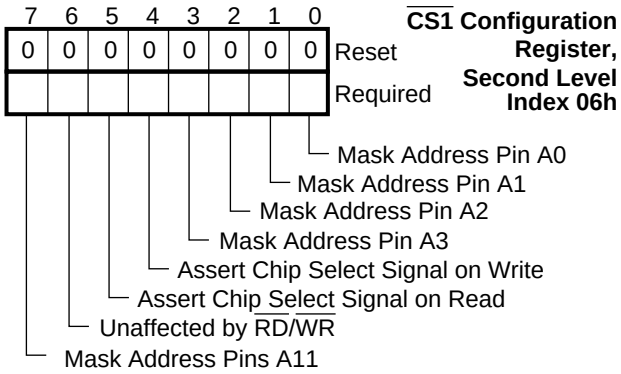


FIGURE 2-12. $\overline{CS1}$ Configuration Register Bitmap

2.10.8 Reserved, Second Level Index 07h

Attempts to access this register produce undefined results.

2.10.9 $\overline{CS2}$ Base Address MSB Register, Second Level Index 08h

This read/write register is reset by hardware to 00h.Same as Plug and Play ISA base address register at index 60h. See Table 2-7 on page 15.

2.10.10 $\overline{CS2}$ Base Address LSB Register, Second Level Index 09h

This read/write register is reset by hardware to 00h. Same as the Plug and Play ISA base address register at index 61h. See Table 2-7 on page 15.

2.10.11 $\overline{CS2}$ Configuration Register, Second Level Index 0Ah

This read/write register is reset by hardware to 00h. Same as $\overline{CS0}$ Configuration register.

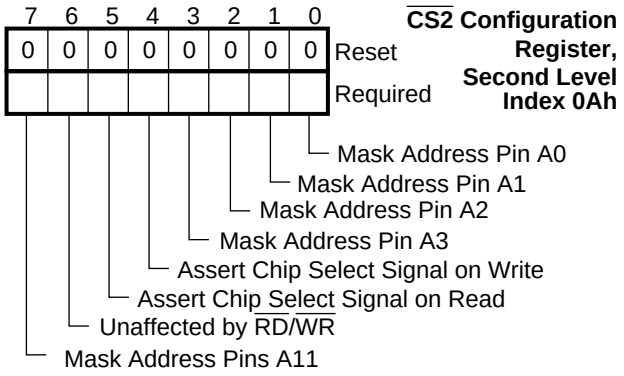


FIGURE 2-13. $\overline{CS2}$ Configuration Register Bitmap

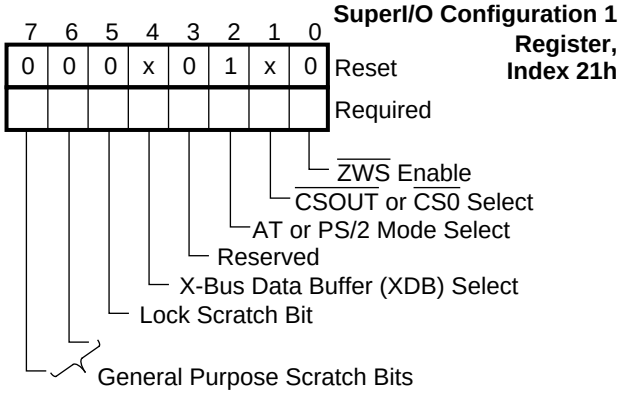
2.10.12 Reserved, Second Level Indexes 0Bh-0Fh

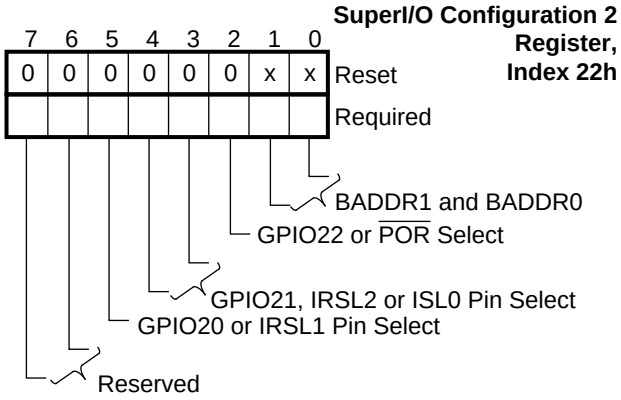
Attempts to access these registers will produce undefined results.

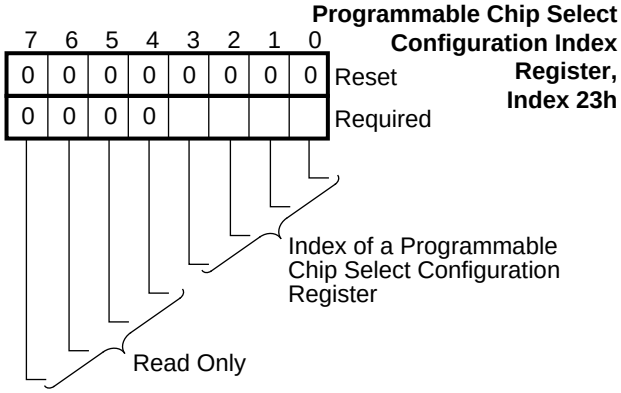
2.10.13 Not Accessible, Second Level Indexes 10h-FFh

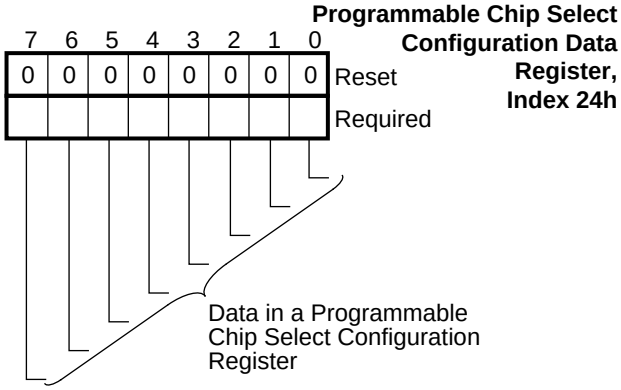
Not accessible because bits 7-4 of the Index register are 0.

2.11 CARD CONTROL REGISTER BITMAPS









SuperI/O KBC Configuration Register, Index F0h

7	6	5	4	3	2	1	0	
0	1	0	0	0	0	0	0	Reset
								Required

- Reserved
- KBC Clock Source

SuperI/O UART1,2 Configuration Register, Index F0h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- TRI-STATE Control for UART Pins
- Power Mode Control
- Busy Indicator/Reserved in UART1
- Ring Detection on $\overline{RI}$ Pin
- Reserved
- Bank Select Enable

SuperI/O FDC Configuration Register, Index F0h

7	6	5	4	3	2	1	0	
0	0	1	0	0	0	0	0	Reset
								Required

- TRI-STATE Control
- Reserved
- DENSEL Polarity Control
- Enhanced TDR Mode
- Four Drive Control

$\overline{CS0}$ Configuration Register, Second Level Index 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- Mask Address Pin A0
- Mask Address Pin A1
- Mask Address Pin A2
- Mask Address Pin A3
- Assert Chip Select Signal on Write
- Assert Chip Select Signal on Read
- Unaffected by $\overline{RD}/\overline{WR}$
- Mask Address Pins A11-4

Drive ID Register, Index F1h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- Drive 0 ID
- Drive 1 ID
- Reserved

$\overline{CS1}$ Configuration Register, Second Level Index 06h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- Mask Address Pin A0
- Mask Address Pin A1
- Mask Address Pin A2
- Mask Address Pin A3
- Assert Chip Select Signal on Write
- Assert Chip Select Signal on Read
- Unaffected by $\overline{RD}/\overline{WR}$
- Mask Address Pins A11-4

SuperI/O Parallel Port Configuration Register, Index F0h

7	6	5	4	3	2	1	0	
1	1	1	1	0	0	1	0	Reset
								Required

- TRI-STATE Control
- Clock Enable
- Reserved
- PP of PnP ISA Resource Data
- Configuration Bits within the Parallel Port
- Parallel Port Mode Select

$\overline{CS2}$ Configuration Register, Second Level Index 0Ah

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- Mask Address Pin A0
- Mask Address Pin A1
- Mask Address Pin A2
- Mask Address Pin A3
- Assert Chip Select Signal on Write
- Assert Chip Select Signal on Read
- Unaffected by $\overline{RD}/\overline{WR}$
- Mask Address Pins A11-4

3.0 Keyboard (and Mouse) Controller (KBC) (Logical Devices 0 and 1)

The Keyboard Controller (KBC) is a functionally independent programmable device controller. It is implemented physically as a single hardware module on the PC87308VUL multi-I/O chip and houses two separate logical devices: a keyboard controller and a mouse controller.

The KBC accepts user input from the keyboard or mouse, and transfers this input to the host PC via the common PC87308VUL-PC interface.

The KBC is functionally equivalent to the industry standard 8042A keyboard controller, which may serve as a detailed technical reference for the KBC.

The KBC is delivered preprogrammed with customer-supplied code. KBC firmware code is identical to 8042 code, and to code of the keyboard controller of the PC87323VUL chip. The PC87323VUL is recommended as a development platform for the KBC since it uses identical code and includes an internal program RAM that enables software development.

3.1 SYSTEM ARCHITECTURE

The KBC is a general purpose microcontroller, with an 8-bit internal data bus. See Figure 3-1. It includes the following functional blocks:

Serial Open-Collector Drivers: Four open-collector bi-directional serial lines enable serial data exchange with the external devices (keyboard and mouse) using the PS/2 protocol.

Program ROM: 2 Kbytes of ROM store program machine code in non-erasable memory. The code is copied to this ROM during manufacture, from customer-supplied code.

Data RAM: 256 bytes of Data RAM enables run-time internal data storage, and includes an 8-level stack and 16 8-bit registers.

Timer/Counter: An internal 8-bit timer/counter can count external events or pre-divided system clock pulses. An internal time-out interrupt may be generated by this device.

I/O Ports: Two 8-bit ports (Port 1 and Port 2) serve various I/O functions. Some are for general purpose use, others are utilized by the KBC firmware as shown in Figure 3-1.

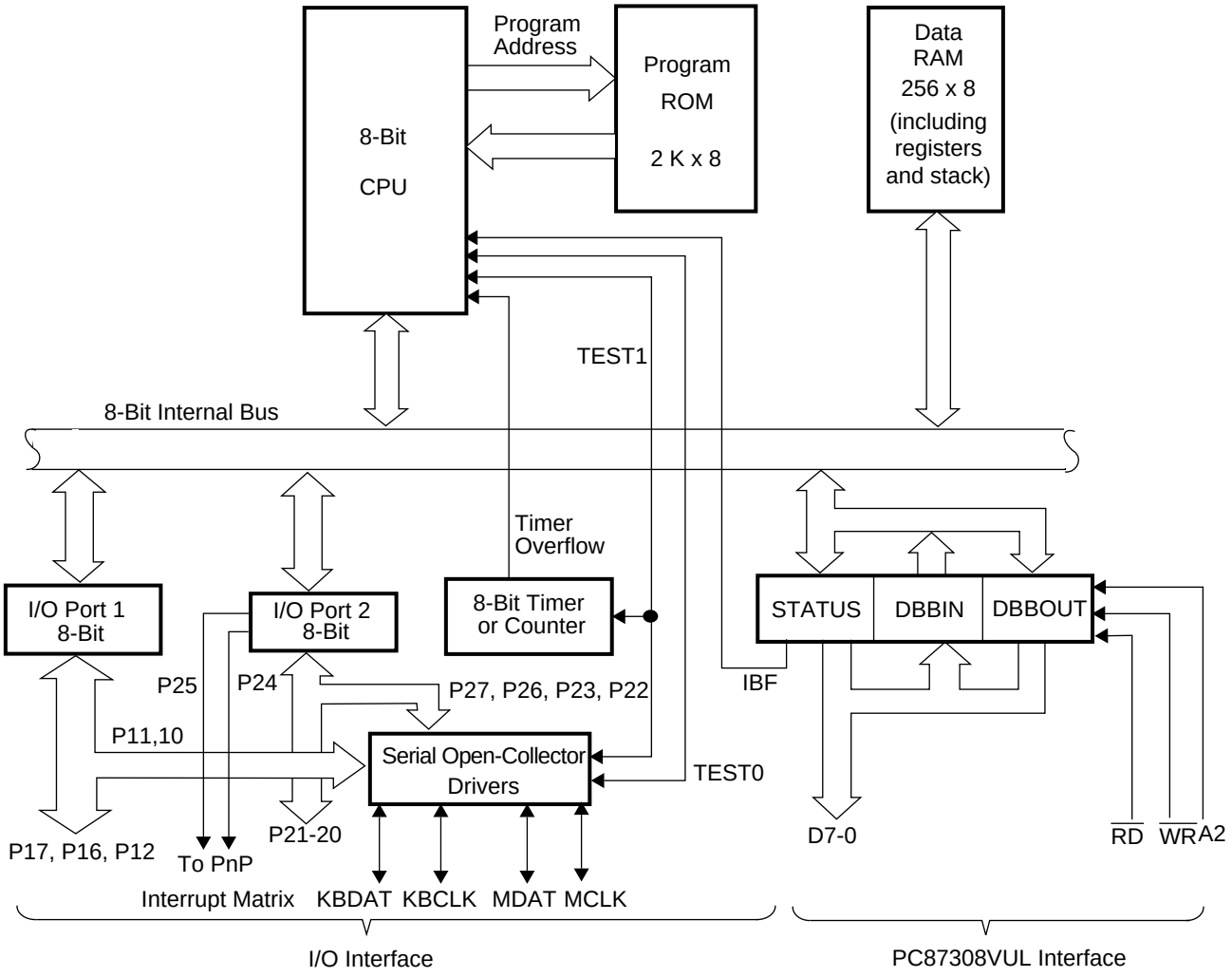


FIGURE 3-1. KBC System Functional Block Diagram

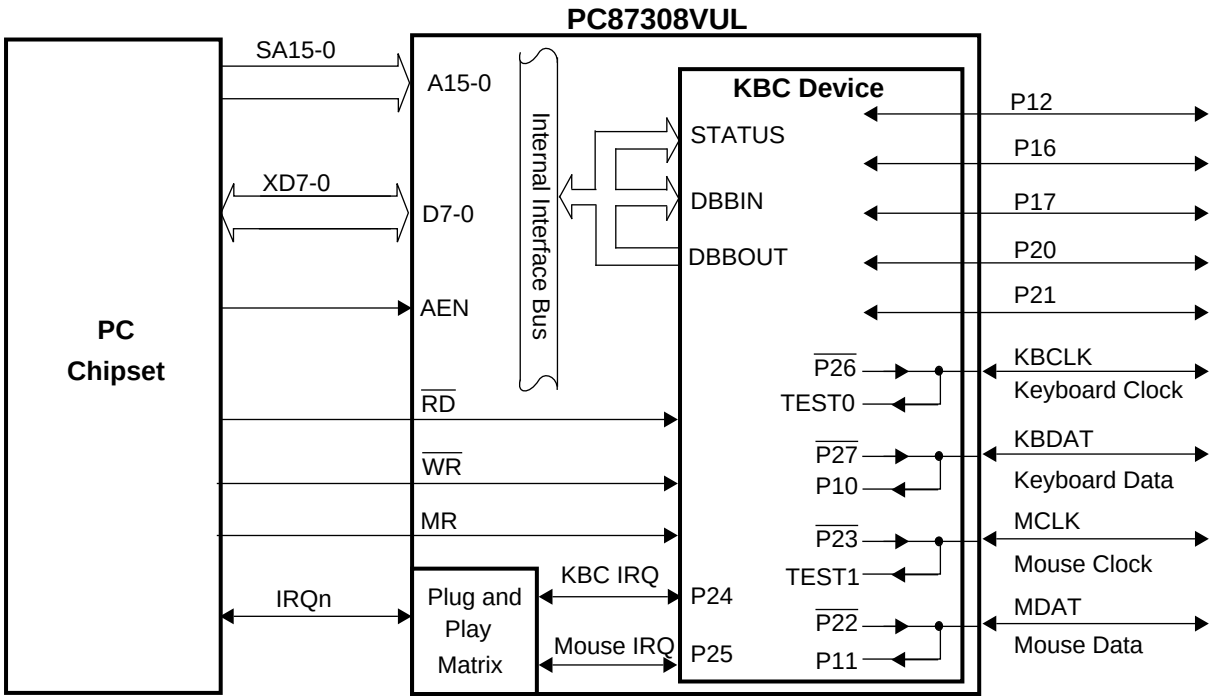


FIGURE 3-2. System Interfaces

3.2 FUNCTIONAL OVERVIEW

The KBC supports two external devices — a keyboard and a mouse. Each device communicates with the KBC via two bidirectional serial signals. Five additional external general-purpose I/O signals are provided.

KBC operation involves three signal interfaces:

- External I/O interface
- Internal KBC - PC87308VUL interface
- PC87308VUL - PC chipset interface.

These system interfaces are shown in Figure 3-2.

The KBC uses two data registers (for input and output) and a status register to communicate with the PC87308VUL central system. Data exchange between these units may be based on programmed I/O or interrupt-driven.

The KBC has two internal interrupts: the Input Buffer Full (IBF) interrupt and Timer Overflow interrupt (see Figure 3-1). These two interrupts can be independently enabled or disabled by KBC firmware. Both are disabled by a hard reset. These two interrupts only affect the execution flow of the KBC firmware, and have no connection with the external interrupts requested by this logical device.

The KBC can generate two external interrupt requests. These request signals are controlled by the KBC firmware which generates them by manipulating I/O port signals. See Section 3.3.2.

The PC87308VUL supports the KBC and handles interactions with the PC chip set. In addition to data transfer, these interactions include KBC configuration, activation and status monitoring. The PC87308VUL interconnects with the host via one interface that is shared by all chip devices.

The KBC clock is generated from the main clock of the chip, which may come from an external clock source or from the internal frequency multiplier. (See Sections 3.3 and 3.4.)

The KBC clock rate is configured by the SuperI/O (SIO) Configuration Registers.

3.3 DEVICE CONFIGURATION

The KBC hardware contains two logical devices—the KBC (logical device 0) and the mouse (logical device 1).

3.3.1 I/O Address Space

The KBC has two I/O addresses and one IRQ line (KBC IRQ) and can operate without the companion mouse. The mouse, however, cannot operate without the KBC device. It has one IRQ line (mouse IRQ) but has no I/O address. It utilizes the KBC I/O addresses.

3.3.2 Interrupt Request Signals

The KBC IRQ and Mouse IRQ interrupt request signals are identical to (or functions of) the P24 and P25 signals of the 8042. These interrupt request signals are routed internally to the Plug and Play interrupt Matrix and may be routed to user-programmable IRQ pins. Each logical device is independently controlled.

The Interrupt Select registers (index 70h for each logical device) select the IRQ pin to which the corresponding interrupt request is routed. The interrupt may also be disabled by not routing its request signal to any IRQ pin.

Bit 0 of the Interrupt Type registers (index 71h for each logical device) determines whether the interrupts are passed (bit 0 = 0) or latched (bit 0 = 1). If bit 0 = 0, interrupt request signals (P24 and P25) are passed directly to the selected IRQ pin. If bit 0 = 1, interrupt request signals that become active are latched on their rising edge, and held until read from the KBC output buffer (port 60h). Figure 3-3 illustrates the internal interrupt request logic.

Note:

The EN FLAGS command (used for routing OBF and IBF onto P24 and P25 in the 8042) causes unpredictable results and should not be issued.

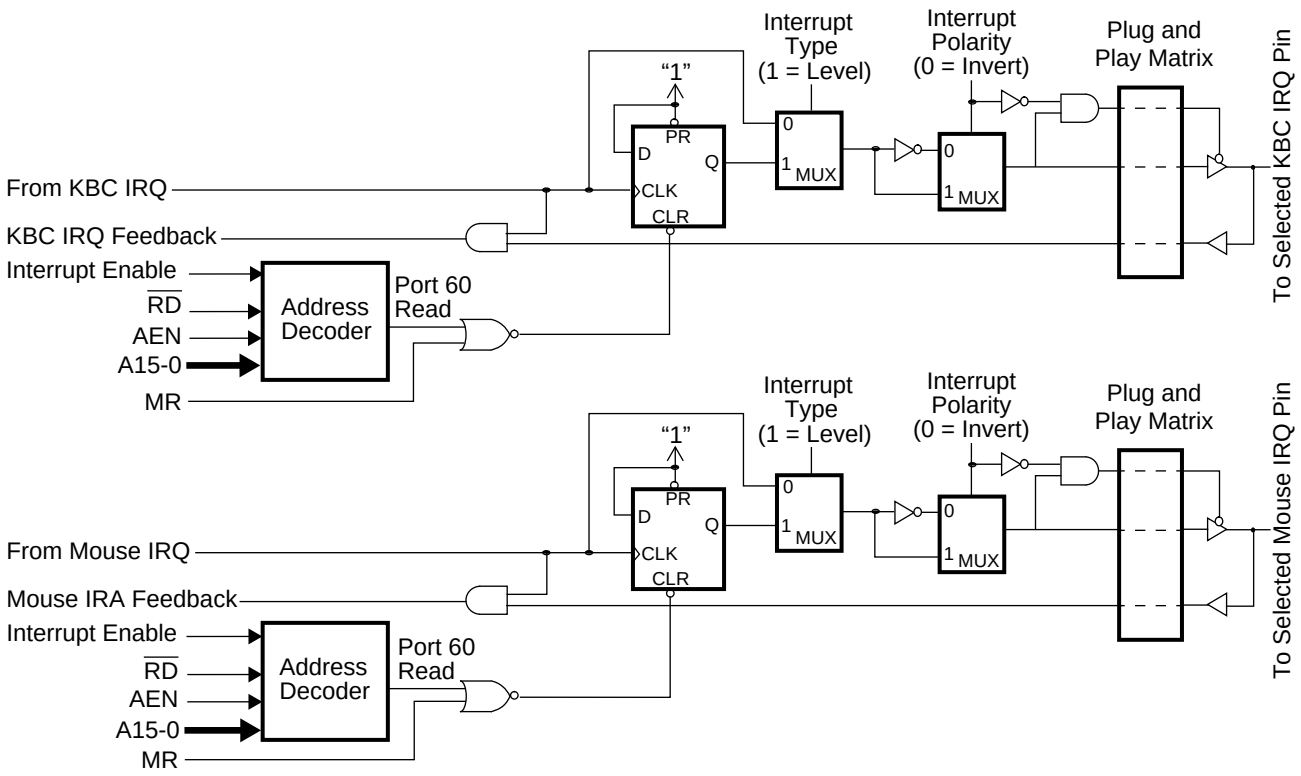


FIGURE 3-3. Interrupt Request Logic

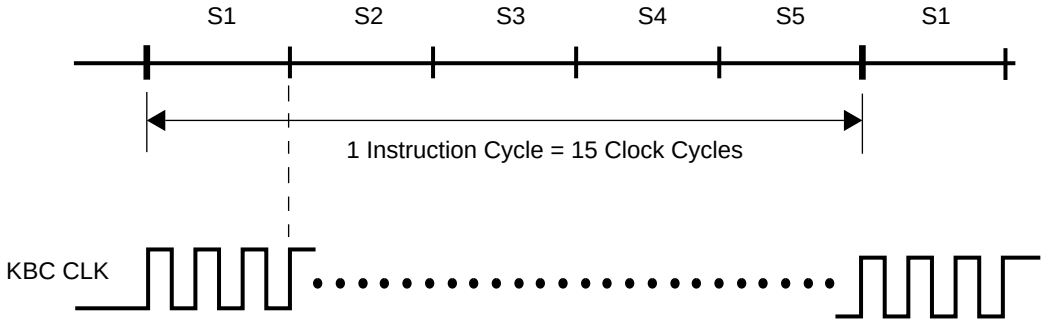


FIGURE 3-4. Instruction Timing

3.3.3 KBC Clock

The KBC clock frequency is selected by the SuperI/O KBC Configuration Register at index F0h of logical device 0 to be either 8, 12 or 16 MHz. 16 MHz is not available when the clock source on pin X1 is 24 MHz. This clock is generated from a 32.768 KHz crystal connected to pins X1C and X2C, or from either a 24 MHz or a 48 MHz clock input at pin X1. See "SuperI/O KBC Configuration Register, Index F0h" on page 23, and Figures 3-4 and 3-5. The clock source and frequency may only be changed when the KBC is disabled.

For details regarding the configuration of each device, refer to Tables 2-12 and 2-13 starting on page 17.

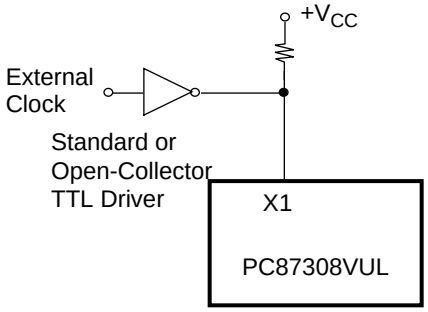


FIGURE 3-5. External Clock Connection

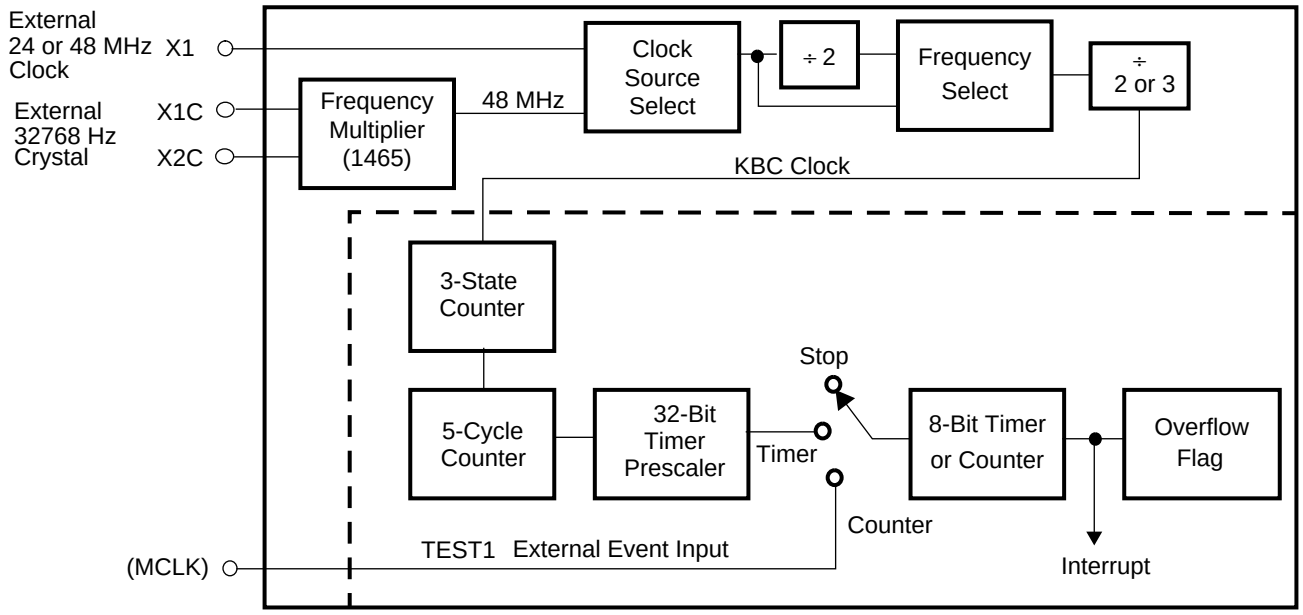


FIGURE 3-6. Timing Generation and Timer Circuit

3.3.4 Timer or Event Counter

The keyboard controller includes an 8-bit counter, which can be used as a timer or an event counter, as selected by the firmware.

Timer Operation

When the internal clock is chosen as the counter input, the counter functions as a timer. The clock fed to the timer consists of the KBC instruction cycle clock, divided by 32. (See Figures 3-4 and 3-6.) The divisor is reset only by a hardware reset or when the timer is started by an STRT T instruction.

The timer counts up from a programmable initial value and sets an overflow flag when it overflows. This flag may be tested, or may be set up to generate an overflow interrupt.

Refer to the 8042 or PC87323VUL instruction set for details.

Event Counter Operation

When the clock input of the counter is switched to the external input (MCLK), it becomes an event counter. The falling edge of the signal on the MCLK pin causes the counter to increment. Timer Overflow Flag and Timer interrupt operate as in the timer mode.

3.4 EXTERNAL I/O INTERFACES

The PC chip set interfaces with the PC87308VUL as illustrated in Figure 3-2 on page 30.

All data transactions between the KBC and the PC chip set are handled by the PC87308VUL.

The PC87308VUL decodes all I/O device chip-select functions from the address bus. The KBC chip-select codes are, traditionally, 60h or 64h, as described in Table 3-1 . (These addresses are user-programmable.)

The external interface includes two sets of signals: the keyboard and mouse interface signals, and the general-purpose I/O signals.

3.4.1 Keyboard and Mouse Interface

Four serial I/O signals interface with the external keyboard and mouse. These signals are driven by open-collector drivers with signals derived from two I/O ports residing on the internal bus. Each output can drive 16 mA, making them suitable for driving the keyboard and mouse cables. The signals are named KBCLK, KBDAT, MCLK and MDAT, and they are the logical complements of P26, P27, P23 and P22, respectively.

TEST0 and TEST1 are dedicated test pins, internally connected to KBCLK and MCLK, respectively, as shown in Figures 3-1 and 3-2. These pins may be used as logical conditions for conditional jump instructions, which directly check the logical levels at the pins.

KBDAT and MDAT are connected to pins P10 and P11, respectively.

MCLK also provides input to the event counter.

3.4.2 General Purpose I/O Signals

The P12, P16, P17, P20 and P21 general purpose I/O signals interface to two I/O ports (port1 and port2). P12, P16 and P17 are mapped to port 1 and P20 and P21 are mapped to port 2.

P12, P16 and P17 are driven by quasi-bidirectional drivers. (See Figure 3-7.) These signals are called quasi-bidirectional because the output buffer cannot be turned off (even when the I/O signal is used for input).

During output, a 1 written to output is strongly pulled up for the duration of a (short) write pulse, and thereafter maintained by a high impedance “weak” active pull-up (implemented by a degenerated transistor employed as a switchable pull-up resistor). A series resistor to those port lines used for input is recommended to limit the surge current during the strong pull-up. See Figure 3-8.

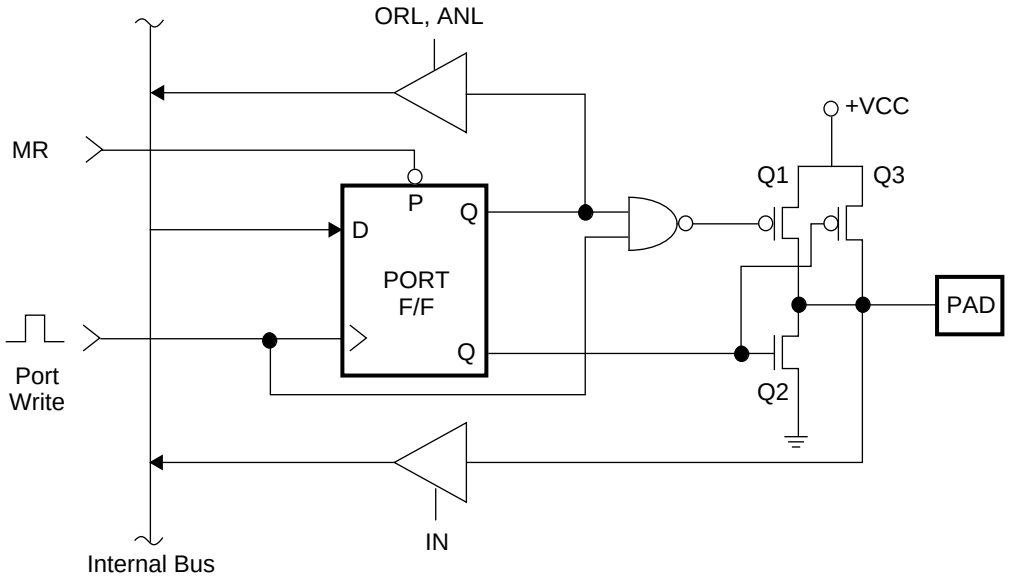


FIGURE 3-7. Quasi-Bidirectional Driver

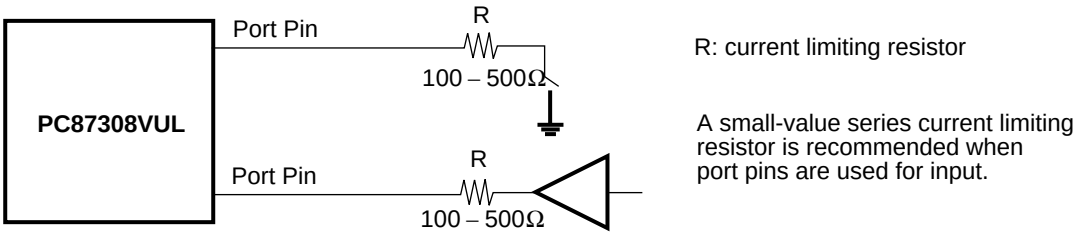


FIGURE 3-8. Current Limiting Resistor

If a 1 is asserted, an externally applied signal may pull down the output. Therefore, input from this quasi-bidirectional circuit can be correctly read if preceded by a 1 written to output.

P20 and P21 are driven by open-drain drivers.

When the KBC is reset, all port data bits are initialized to 1.

3.5 INTERNAL KBC - PC87308VUL INTERFACE

The KBC interfaces internally with the PC87308VUL via three registers: an input (DBBIN), output (DBBOUT) and status (STATUS) register. See Figure 3-1 on page 29 and Table 3-1.

TABLE 3-1. System Interface Operations

$\overline{RD}$	$\overline{WR}$	Default Addresses	Operation
0	1	60h	Read DBBOUT
1	0	60h	Write DBBIN, F1 Clear (Data)
0	1	64h	Read STATUS
1	0	64h	Write DBBIN, F1 Set (Command)

Table 3-1 illustrates the use of address line A2 to differentiate between data and commands. The device is selected by chip identification of default address 60h (when A2 is 0) or 64h (when A2 is 1). After reset, these addresses can be changed by software.

3.5.1 The KBC DBBOUT Register, Offset 60h, Read Only

The DBBOUT register transfers data from the keyboard controller to the PC87308VUL. It is written to by the keyboard controller and read by the PC87308VUL for transfer to the PC. The PC may be notified of the need to read data from the KBC by an interrupt request or by polling the Output Buffer Full (OBF) bit (bit 0 of the KBC STATUS register described in Section 3.5.3 on page 34).

3.5.2 The KBC DBBIN Register, Offset 60h (F1 Clear) or 64h (F1 Set), Write Only

The DBBIN register transfers data from the PC87308VUL system to the keyboard controller. (This transaction is transparent to the user, who should program the device as if direct access to the registers were in effect.)

When data is received in this manner, an Input Buffer Full (IBF) internal interrupt may be generated in the KBC, to deal with this data. Alternatively, reception of data in this manner can be detected by the KBC polling the Input Buffer Full bit (IBF, bit 1 of the KBC STATUS register).

3.5.3 The KBC STATUS Register, Offset 64h, Read Only

The STATUS register holds information regarding the system interface status. Figure 3-9 shows the bit definition of this register. This register is controlled by the KBC firmware and hardware, and is read-only for the system.

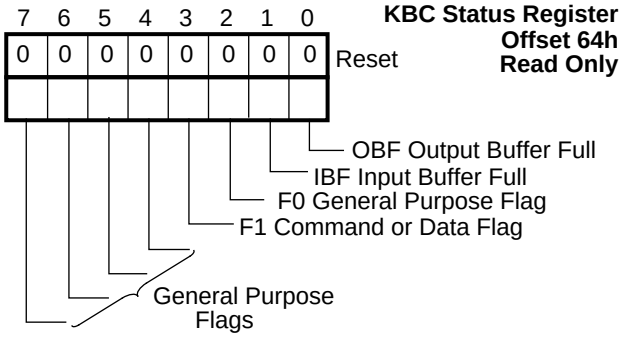


FIGURE 3-9. KBC STATUS Register Bitmap

Bit 0 - OBF, Output Buffer Full

A 1 indicates that data has been written into the DBBOUT register by the KBC. It is cleared by a system read operation from DBBOUT.

Bit 1 - IBF, Input Buffer Full

When a write operation is performed by the host system, this bit is set to 1, which may be set up to trigger the IBF interrupt. Upon executing an IN A, DBB instruction, it is cleared.

Bit 2 - F0, General Purpose Flag

A general purpose flag that can be cleared or toggled by the keyboard controller firmware.

Bit 3 - F1, Command/Data Flag

This flag holds the state of address line A2 while a write operation is performed by the host system. It distinguishes between commands and data from the host system. In this device, a write with A2 = 1 (hence F1 = 1) is defined as a command, and A2 = 0 (hence F1 = 0) is data.

Bits 7-4, General Purpose Flags

These flags may be modified by KBC firmware.

3.6 INSTRUCTION TIMING

The KBC clock is first divided by 3 to generate the state timing, then by 5 to generate the instruction timing. Thus each instruction cycle consists of five states and 15 clock cycles.

Most keyboard controller instructions require only one instruction cycle, while some require two cycles. Refer to the 8042 or PC87323VUL instruction set for details.

4.0 Real-Time Clock (RTC) and Advanced Power Control (APC) (Logical Device 2)

The RTC logical device contains two major functions: the Real-Time Clock (RTC) and Advanced Power Control (APC).

The RTC is a timekeeping module that supplies a time-of-day clock and a multi-century calendar in various formats. It provides alarm facilities and three programmable timer interrupts. It continues valid timekeeping and maintains RAM contents during power down by utilizing external battery backup.

Additional features of the PC87308VUL RTC include Advanced Power Control (APC), a century timekeeping storage byte, full Plug and Play support, additional battery-backed RAM and RAM lock schemes, and additional power management options.

The APC function adds the ability of automatic PC system power-up in response to external events. This enables efficient use of the PC system in applications such as voice answering machines or fax receivers, which are typically powered up at all times.

The APC also enables a controlled power-down sequence when switched off by the user. The APC function does not replace the power management abilities of various PC87308VUL modules–it adds power management ability to the PC host system.

RTC software is compatible with the DS1287 and MC146818 clock chips. (The only difference is that Port 70 is read/write in this module, and is write-only in the DS1287 and MC146818.)

Battery-Backed Register Banks and RAM

The RTC and APC module has three battery-backed register banks. Two are used by the logical units themselves. The host system uses the third for general purpose battery-backed storage.

Battery-backup power enables information retention during system power down.

The banks are:

- Bank 0 - General Purpose Register Bank
- Bank 1 - RTC Register Bank
- Bank 2 - APC Register Bank

The memory maps and register content for each of the three banks is illustrated in Section 4.7 on page 50.

The lower 64-byte locations of the three banks are shared. The first 14 bytes store time and alarm data and contain control registers. The next 50 bytes are general purpose memory.

The upper 64 bytes of bank addresses are utilized as follows:

- Bank 0 supplies an additional 64 bytes of memory backed RAM.
- Bank 1 uses the upper 64 bytes for functions specific to the RTC activity and for addressing Upper RAM.
- Bank 2 uses the upper 64 bytes for functions specific to the APC activity.

Registers with reserved bits should be written in “Read-Modify-Write” method.

RTC Control Register A (CRA) selects the active bank according to the value of bits 6-4 (DV2-0). (See Table 4-3 on page 39.)

All register locations within the device are accessed by the RTC Index and Data registers (at base address and base address+1). The Index register points to the register location being accessed, and the Data register contains the data to be transferred to or from the location. An additional 128 bytes of battery-backed RAM (also called upper RAM) may be accessed via a second level address. The second level uses the upper RAM Index register at index 50h of bank 1 and the upper RAM Data register at index 53h of bank 1.

Access to the three register banks and RAM may be locked. For details see “RAM Lock Register (RLR), Index 47h” on page 48.

4.1 RTC OPERATION OVERVIEW

The control registers listed in Table 4-1 control all RTC operation. These registers appear in all the RTC register banks. See Section 4.7 on page 50.

TABLE 4-1. RTC Control Registers

Index	Name	Description
0Ah	CRA	RTC Control Register A
0Bh	CRB	RTC Control Register B
0Ch	CRC	RTC Control Register C
0Dh	CRD	RTC Control Register D

RTC configuration registers within the PC87308VUL store the settings for all interface, configuration and power management options. These registers are described in detail in Section 2.3 on page 13.

The RTC employs an external crystal connected to an internal oscillator circuit or an optional external clock input, as the basic clock for timekeeping.

Local battery-backed RAM serves as storage for all timekeeping functions.

4.1.1 RTC Hardware and Functional Description

Bus Interface

The RTC function is initially mapped to the default I/O locations at indexes 70h (Index) and 71h (data) within the PC87308VUL. These locations may be reassigned, in compliance with the Plug and Play requirements. See Section 2.2 on page 12.

External Clock and Timing Generation

The RTC can use one of the following timekeeping input clock options:

- A 32768 Hz crystal connected externally at the X1C and X2C pins completes an oscillator circuit and generates the 32768 Hz input clock. (See “Oscillator Internal and External Circuitry” on page 36.)

- An external clock may be connected to pin X1C.

The time generation function divides the 32.768 KHz by 2^{15} to derive a 1 Hz signal which serves as the input for timekeeping functions. Bits 6-4 of RTC Control Register A (CRA) control the activity and location of the divider chain in memory. Bits 3-0 of the CRA register select one of fifteen taps from the divider chain to be used as a periodic interrupt. See Section “RTC Control Register A (CRA), Index 0Ah” on page 38 for a description of divider configurations and rate selections.

The divider chain is reset to 0 by bits 6-4 of the CRA register. An update occurs 500 msec after the divider chain is activated by setting normal operational mode (bits 6-4 of CRA = 010). The periodic flag becomes active one half of the programmed period after the divider chain is activated.

Figure 4-1 illustrates the internal and external circuitry that comprise the oscillator.

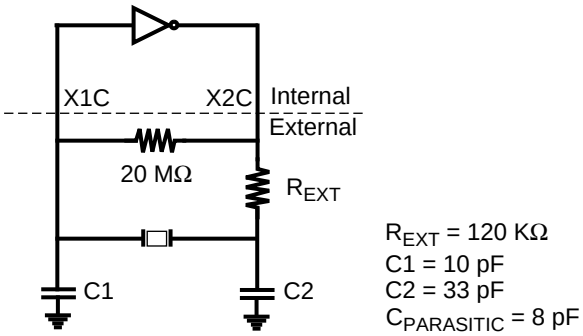


FIGURE 4-1. Oscillator Internal and External Circuitry

This oscillator is active under normal power or during power down. It stops only in the event of a power failure with the oscillator disabled (see “Oscillator Activity” on page 38), or when battery backup power drops below two volts.

If oscillator input is from an external source, input should be driven rail to rail and should have a nominal 50% duty cycle. In this case, oscillator output X2C should be disabled.

External capacitor values should be chosen to provide the manufacturer’s specified load capacitance for the crystal when combined with the parasitic capacitance of the trace, socket, and package, which can vary from 0 to 8 pF. The rule of thumb in choosing these capacitors is:

$C_L = (C1 * C2) \div (C1 + C2) + C_{PARASITIC}$

$C2 > C1$

C1 can be trimmed to achieve precisely 32768.0 Hz after insertion.

Start-up time for this oscillator may vary from two to seven seconds due to the high Q of the crystal. The parameters below describe the crystal requirements:

Parallel, resonant, tuning fork (N cut) or XY bar

$Q \geq 35000$

Load Capacitance (C_L) 9 to 13 pF

Accuracy and temperature coefficients are user defined.

4.1.2 Timekeeping

Time is kept in BCD or binary format as determined by bit 2 (DM) of Control Register B (CRB). Either 12 or 24 hour representation for the hours can be maintained as determined by bit 1 of CRB. When changing formats, the time registers must be re-initialized to the corresponding data format.

Daylight savings time and leap year exceptions are handled by the timekeeping function. When bit 0 (the Daylight Saving Enable bit, DSE) of CRB is set to 1, time advances from 1:59:59 AM to 3:00:00 on the first Sunday in April, and changes from 1:59:59 to 1:00:00 on the last Sunday of October. In leap years, February is extended to 29 days.

Updating

Timekeeping is performaed by hardware, which updates a pre-programmed time value once per second. The pre-programmed time values are written by the user to the following locations:

The values for seconds, minutes, hours, day of week, date of month, month and year are located in the common storage area in all three memory banks (See Table 4-6 on page 50). The century value is located in Bank 1 (See Table 4-8 on page 51).

Users must ensure that reading or writing to the time storage locations does not coincide with a system update of these locations, which would cause invalid and unpredictable results.

There are several ways to avoid this contention. Four options follow:

Method 1 - Set the SET bit (bit 7 of the CRB register) to 1.

This takes a “snapshot” of the internal time registers and loads it into the user copy. If user copy registers have been updated, the user copy updates the internal registers when the SET bit goes from 1 to 0. This mechanism enables loading new time parameters into the RTC.

Method 2 - Access after detection of an Update-Ended interrupt.

This implies that an update has just completed and there are 999 msec remaining until the next occurrence.

Method 3 - Poll Update-In-Progress (UIP) (bit 7 in Control Register A).

The update occurs 244 µsec after the update-in-progress bit goes high. Therefore if a 0 is read, there is a minimum of 244µs in which the time is guaranteed to remain stable.

Method 4 - Use a periodic interrupt to determine if an update cycle is in progress.

The periodic interrupt is first set to a desired period. Periodic interrupt appearance then indicates there is a period of (Period of periodic interrupt ÷ 2 + 244 µsec) remaining until another update occurs.

Alarms

The timekeeping function may generate an alarm when the current time reaches a stored alarm time. After each RTC time update, the seconds, minutes, and hours storage locations are compared with the seconds, minutes and hours in the alarm storage locations. If equal, the alarm flag is set in Control Register C (CRC). If the Alarm Interrupt Enable (AIE) bit is set in Control Register B (CRB), then setting the Alarm Flag (AF) in CRC generates the $\overline{IRQ}$ internal interrupt request ($\overline{IRQ}$ = 0).

Any alarm location, i.e., seconds, minutes or hours, may be set to a “Don’t Care” state by setting bits 7,6 to 11. (This value is unused for either BCD or binary time codes.) This results in periodic alarm activation at an increased rate whose period is that of the Don’t Care location, e.g., if the hours location is set to 11, the alarm will be activated every hour.

The seconds, minutes and hours alarm registers are shared with the wake-up function.

4.1.3 Power Management

The host PC and PC87308VUL power is supplied by the system power supply voltage, $V_{DD.}$

Figure 4-2 shows the power supplies of the PC87308VUL.

A trickle voltage (V_{CCH}) from the external AC power supply powers the RTC and APC under normal conditions. The V_{DD} voltage reaches the RTC/APC as a sense signal, to determine the presence or absence of a valid V_{DD} supply.

A battery backup voltage V_{BAT} maintains RTC/APC timekeeping and backup memory storage when the V_{CCH} voltage is absent, due to power failure or disconnection of the external AC input power supply.

The APC function produces the $\overline{ONCTL}$ signal, which controls the V_{DD} power supply voltage. (See Section 4.4.1 on page 44.)

To ensure proper operation, a 500 mV differential is needed between V_{CCH} and V_{BAT}.

Figure 4-3 represents a typical battery configuration. No external diode is required to meet the UL standard, due to the internal serial resistor.

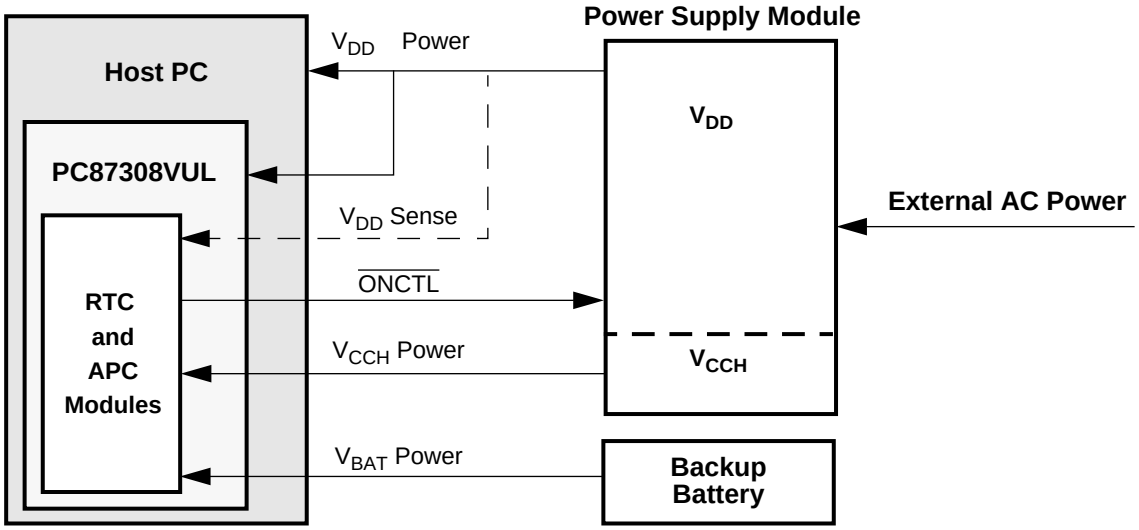


FIGURE 4-2. PC87308VUL Power Supplies

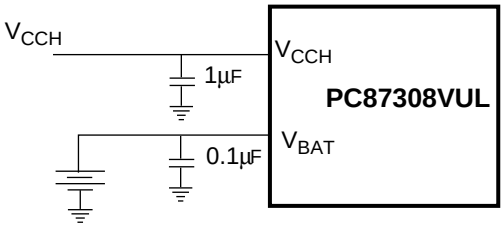


FIGURE 4-3. Typical Battery Configuration

System Bus Lockout

As the RTC switches to battery power all, input signals are locked out so that the internal registers can not be modified externally.

Power Up Detection

When system power is restored after a power failure, the power failure lock condition continues for a delay of 62 msec (minimum) to 125 msec (maximum) after the RTC switches from battery power to system power.

The power failure lock condition is switched off immediately in the following situations:

- If the Divider Chain Control bits (DV2-0, bits 6-4 in Control Register A) specify any mode other than 010, 100 or 011, all input signals are enabled immediately upon detection of system voltage above that of the battery voltage.
- When battery voltage is below 1 volt and MR is 1, all input signals are enabled immediately upon detection of system voltage above that of battery voltage. This also initializes registers at indexes 00h through 0Dh.
- If the VRT bit (bit 7 in Control Register D) is 0, all input signals are enabled immediately upon detection of system voltage above that of battery voltage.

Oscillator Activity

The RTC internal oscillator circuit is active whenever power is supplied to the RTC, unless software wrote 000 or 001 to the Divider Chain Control bits (DV2-0), i.e., bits 6-4, of Control Register A, and the RTC is supplied by V_{BAT} or unless the RTC is supplied by V_{BAT} and the VRT bit of Control Register D is 0. This disables the oscillator.

When the oscillator becomes inactive, the APC is disabled.

4.1.4 Interrupt Handling

The RTC logic device has a single Interrupt Request line, $\overline{IRQ}$, which handles three interrupt conditions. The Periodic, Alarm, and Update-Ended interrupts are generated ($\overline{IRQ}$ is driven low) if the respective enable bits in Control Register B are set when an interrupt event occurs.

Reading RTC Control Register C (CRC) clears all interrupt flags. Thus, it is recommended that when multiple interrupts are enabled, the interrupt service routine should first read and store the CRC register, then deal with all pending interrupts by referring to this stored status.

If an interrupt is not serviced before a second occurrence of the same interrupt condition, the second interrupt event is lost. Figure 4-5 illustrates interrupt and status timing in the PC87308VUL.

4.2 THE RTC REGISTERS

The RTC registers can be accessed at any time during non-battery backed operation. These registers cannot be written to before reading the VRT bit (bit 7 of the “RTC Control Register D (CRD), Index 0Dh” on page 41), thus preventing bank selection and other functions. The user must read the VRT bit as part of the startup activity.

These registers are listed in Table 4-1 and described in detail in the sections that follow.

4.2.1 RTC Control Register A (CRA), Index 0Ah

The CRA register controls periodic interrupt rate selection and bank selection.

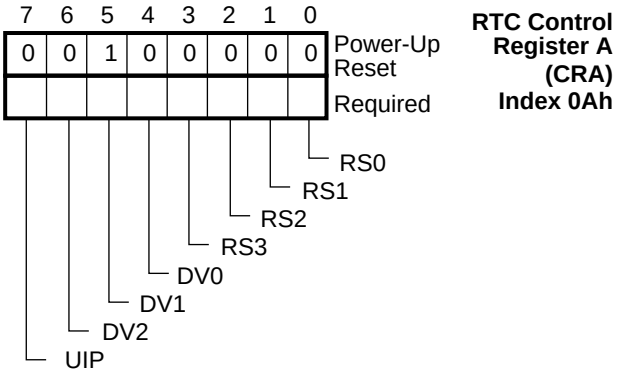


FIGURE 4-4. CRA Register Bitmap

Bits 3-0 - Periodic Interrupt Rate Select (RS3-0)

These read/write bits select one of fifteen output taps from the clock divider chain to control the rate of the periodic interrupt. See Table 4-2 and Figure 4-5.

Master reset does not affect these bits.

Bits 6-4 - Divider Chain Control (DV2-0)

These read/write bits control the configuration of the divider chain for timing generation and memory bank selection, as shown in Table 4-3.

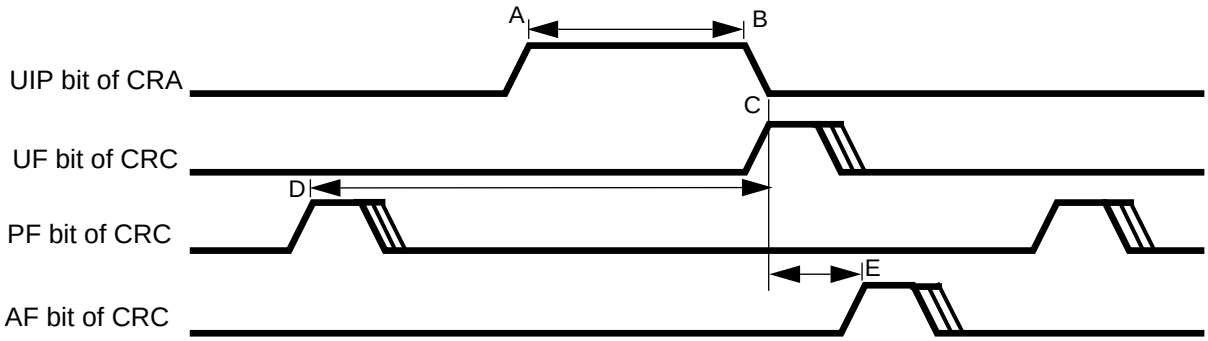
Master reset does not affect these bits.

Bit 7 - Update in Progress (UIP)

This read only bit is not affected by reset.

0 - An update will not occur within the next 244 µsec. Bit 7 (the SET bit) of Control Register B (CRB) is 1.

1 - Timing registers are updated within 244 µsec.



A-B Update In Progress (UIP) bit high before update occurs = 244 µsec
D-C Periodic interrupt to update = Period (periodic int) / 2 + 244 µsec
C-E Update to Alarm Interrupt = 30.5 µs

UIP Update In Progress status bit
UF Update-Ended Interrupt Flag (Update-Ended Interrupt if enabled)
PF Periodic Flag (Periodic Interrupt if enabled)
AF Alarm Flag (Alarm Interrupt if enabled)

Flags (and IRQ) are reset at the conclusion of Control Register C (CRC) read or by reset.

FIGURE 4-5. Interrupt/Status Timing

TABLE 4-2. Periodic Interrupt Rate Encoding

RS3-0 3 2 1 0	Periodic Interrupt Rate	
0 0 0 0	none	
0 0 0 1	3.90625	msec
0 0 1 0	7.8125	msec
0 0 1 1	122.070	µsec
0 1 0 0	244.141	µsec
0 1 0 1	488.281	µsec
0 1 1 0	976.562	µsec
0 1 1 1	1.953125	msec
1 0 0 0	3.90625	msec
1 0 0 1	7.8125	msec
1 0 1 0	15.625	msec
1 0 1 1	31.25	msec
1 1 0 0	62.5	msec
1 1 0 1	125	msec
1 1 1 0	250	msec
1 1 1 1	500	msec

TABLE 4-3. Divider Chain Control and Bank Selection

DV2-0 6 5 4	Selected Bank	Configuration
0 0 0	Bank 0	Oscillator Disabled[a]
0 0 1	Bank 0	Oscillator Disabled[a]
0 1 0	Bank 0	Normal Operation
0 1 1	Bank 1	Normal Operation
1 0 0	Bank 2	Normal Operation
1 0 1	Undefined	Test
1 1 0	Bank 0	Divider Chain Reset
1 1 1	Bank 0	Divider Chain Reset

a. The oscillator stops in this case only in the event of a power failure.

4.2.2 RTC Control Register B (CRB), Index 0Bh

This register enables the selection of various time and date options, as well as the use of interrupts.

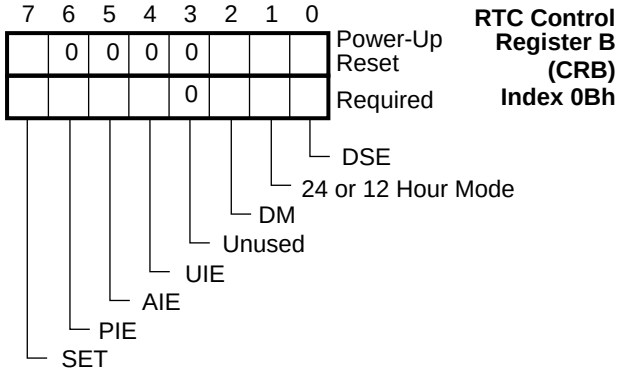


FIGURE 4-6. CRB Register Bitmap

Bit 0 - Daylight Savings Enable (DSE)

Master reset does not affect this read/write bit.

0 - Disables the daylight savings feature.

1 - Enables daylight savings feature, as follows:

In the spring, time advances from 1:59:59 to 3:00:00 on the first Sunday in April.

In the fall, time returns from 1:59:59 to 1:00:00 on the last Sunday in October.

Bit 1 - 24 or 12 Hour Mode

This is a read/write bit that is not affected by reset.

0 - Enables 12 hour format.

1 - Enables 24 hour format.

Bit 2 - Data Mode (DM)

This is a read/write bit that is not affected by reset.

0 - Enables BCD format.

1 - Enables binary format.

Bit 3 - Unused

This bit is defined as “Square Wave Enable” by the MC146818 and is not supported by the RTC. This bit is always read as 0.

Bit 4 - Update-Ended Interrupt Enable (UIE)

Master reset forces this read/write bit to 0.

0 - Disables generation of the Update-Ended interrupt.

1 - Enables generation of the Update-Ended interrupt. This interrupt is generated at the time an update occurs.

Bit 5 - Alarm Interrupt Enable (AIE)

Master reset forces this read/write bit to 0.

0 - Disables generation of the alarm interrupt.

1 - Enables generation of the Alarm interrupt. The alarm interrupt is generated immediately after a time update in which the Seconds, Minutes, and Hours time equal their respective alarm counterparts.

Bit 6 - Periodic Interrupt Enable (PIE)

Master reset forces this read/write bit to 0.

0 - Disables generation of the Periodic interrupt.

1 - Enables generation of the Periodic interrupt. Bits 3-0 of Control Register A (CRA) determine the rate of the Periodic interrupt.

Bit 7 - Set Mode (SET)

Master reset does not affect this read/write bit.

0 - The timing updates occur normally.

1 - The user copy of time is “frozen”, allowing the time registers to be accessed without regard for an occurrence of an update.

4.2.3 RTC Control Register C (CRC), Index 0Ch

This register indicates the status of interrupt request flags.

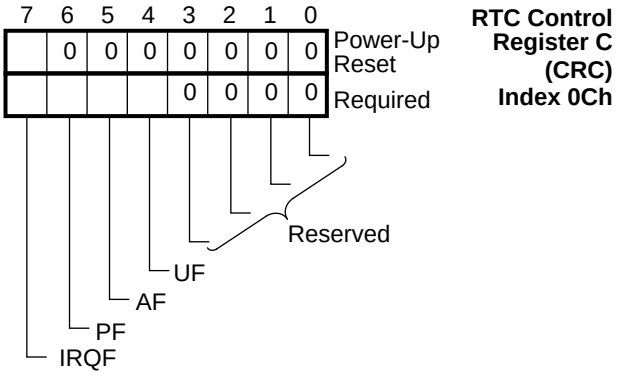


FIGURE 4-7. CRC Register Bitmap

Bits 3-0 - Reserved

These bits are reserved and always return 0000.

Bit 4 - Update-Ended Interrupt Flag (UF)

Master reset forces this read-only bit to 0. In addition, this bit is reset to 0 when this register is read.

0 - No update has occurred since the last read.

1 - Time registers have been updated.

Bit 5 - Alarm Interrupt Flag (AF)

Master reset forces this read-only bit to 0.

0 - No alarm was detected since the last read.

1 - An alarm condition was detected. This bit is reset to 0 when this register is read.

Bit 6 - Periodic Interrupt Flag (PF)

Master reset forces this read-only bit to 0. In addition, this bit is reset to 0 when this register is read.

0 - Indicates no transition occurred on the selected tap since the last read.

1 - A transition occurred on the selected tap of the divider chain.

Bit 7 - Interrupt Request Flag (IRQF)

This read-only bit is the inverse of the value on the $\overline{IRQ}$ output signal of the RTC/APC.

0 - $\overline{IRQ}$ is inactive (high).

1 - $\overline{IRQ}$ is active (low) and any of the following conditions exists: both PIE and PF are 1; both AIE and AF are 1; both UIE and UF are 1. (PIE, AIE and UIE are bits 6, 5 and 4, respectively of the CRB register.)

4.2.4 RTC Control Register D (CRD), Index 0Dh

This register indicates the validity of the RTC RAM data.

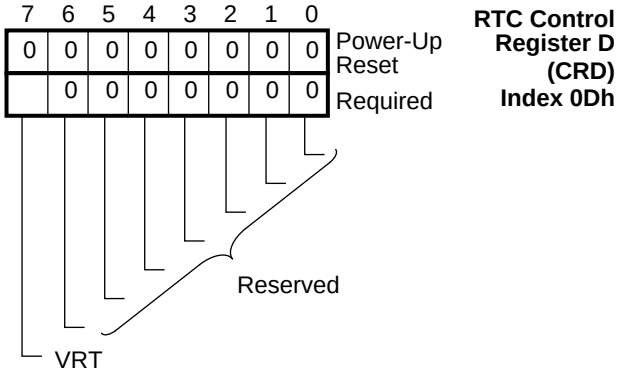


FIGURE 4-8. CRD Bitmap

Bits 6-0 - Reserved

These bits are reserved and are always 0.

Bit 7 - Valid RAM and Time (VRT)

The VRT bit senses the voltage that feeds this logical device (V_{CCH} or V_{BAT}) and indicates whether or not it was too low since the last time this bit was read. If it was too low, the RTC and RAM data are not valid.

This read-only bit is set to 1 when this register is read.

0 - The voltage that feeds the APC/RTC logical device was too low.

1 - The RTC and RAM data are valid.

WARNING:

If V_{DD} ramps down at a rate exceeding 1 V/msec, it may reset this bit.

4.3 APC OVERVIEW

Advanced Power Supply Control (APC) is implemented within the RTC logical device. It enables the PC to power up automatically, as required by specific conditions, or to power down in an orderly, controlled manner, replacing the physical power supply On/Off switch.

The APC device is powered at all times that external AC power or battery backup power are connected to the RTC device. This is true even though the PC may be switched off or disconnected from the external AC power outlet, in which case the APC device is active but does not activate system power. The APC device powers up the entire PC system upon the occurrence of various events (including the power-on switch event).

WARNING:

The APC device does not function if the 32.768 KHz oscillator is not running.

The APC function produces the $\overline{ONCTL}$ signal to activate the system power supply, and the Power-Off Request ($\overline{POR}$) interrupt request signal when there is a request for power off.

$\overline{ONCTL}$: The $\overline{ONCTL}$ signal physically activates or deactivates the system power supply.

The $\overline{ONCTL}$ value depends on the following:

- External events
- Programmable parameter settings
- The system state when an external event occurs
- The state of the system power supply.

$\overline{POR}$: The APC generates a Power-Off Request ($\overline{POR}$) interrupt request signal when the power switch is manually toggled to turn the power off. This enables a software controlled exit procedure (analogous to the **`autoexec.bat`** startup procedure in DOS operating systems) with automatic activation of preprogrammed features such as system status backup, system activity logging, file closing and backup, remote communications termination, print completion, etc.

Table 4-4 shows the registers used for Automatic Power Supply Control (APC) in the PC87308VUL.

TABLE 4-4. APC Control Register List

Index	Mnemonic	Description
40h	APCR1	APC Control Register 1
41h	APCR2	APC Control Register 2
42h	APSR	APC Status Register
47h	RLR	RAM Lock Register

4.3.1 User Selectable Parameters

The APC function enables users to tailor system response to power up, power down, power failure and battery operation situations.

User-selectable parameters include:

- Enabling various external events to wake up the system. See “Power Up” on page 44.
- Wake-up time for an automatic system wake-up. See “Predetermined Wake-Up” on page 46.

- Type of system recovery after a Power Failure state by setting the MOAP bit. See page “The MOAP Bit” on page 44.
- Immediate or delayed Switch Off shutdown. See “The SWITCH Input Signal” on page 45.
- 5 or 21 second time-out fail-safe shutdown. See “The SWITCH Input Signal” on page 45.

4.3.2 System Power States

The system power state may be No Power, Power On, Power Off or Power Failure. These states are illustrated in Figure 4-9 on page 43. Table 4-5 indicates the power-source combinations for each state. No other power-source combinations are valid.

In addition, the power sources and distribution for the entire PC system are described in “PC87308VUL Power Supplies” on page 37.

TABLE 4-5. System Power States

V_{DD}	V_{CCH}	V_{BAT}	Power State
–	–	–	No Power
–	–	+	Power Failure
–	+	+ or -	Power Off
+	+	+ or -	Power On
+	–	+	Illegal State

WARNING:

a. If V_{DD} ramps down at a rate exceeding 1 V/msec, it may reset the Valid RAM and Time (VRT) bit (bit 7) of CRD.

b. It is illegal for V_{DD} to be present when V_{CCH} is absent.

No Power

This state exists when no external or battery power is connected to the device. This condition will not occur once a backup battery has been connected, except in the case of a malfunction. The APC undergoes initialization only when leaving this state.

Power On

This is the normal state when the PC is active. This state may be initiated by various events in addition to the normal physical switching on of the system. In this state, the PC power supply is powered by external AC power and produces V_{DD} and V_{CCH}. The PC system and the PC87308VUL device are powered by $V_{DD,}$ with the exception of the RTC logical device, which is powered by $V_{CCH.}$

Power Off (Suspended)

This is the normal state when the PC has been switched off and is not required to be active, but is still connected to a live external AC input power source. This state may be initiated directly or by software. The PC system is powered down. The RTC logical device remains active, powered by V_{CCH}.

Power Failure

This state occurs when the external power source to the PC stops supplying power, due to disconnection or power failure on the external AC input power source. The RTC continues to maintain timekeeping and RAM data under battery power (V_{BAT}), unless the oscillator stop bit was set in the RTC. In this case, the oscillator stops functioning if the system goes to battery power, and timekeeping data becomes invalid.

4.3.3 System Power Switching Logic

In the Power On state, the PC host is powered by the power-supply voltage V_{DD}. From this state the system enters the Power Off state, if the conditions for this state occur (See Section 4.4.3), or the Power Failure state if external power is removed.

In the Power Off state, the PC hosts do not receive power from the system power supply, except for RTC and APC which receive $V_{CCH.}$ The system may enter the Power On state if the conditions for this state occur (see Section 4.4.3), or enter the Power Failure state if external power is removed.

If the system voltage falls to the level of V_{BAT} +500 mvolt or less, the APC enters the Power Failure state and switches to battery power.

When power returns after a power failure, the APC enables power up after a delay of 1 second. The nature of the power up depends on the MOAP bit setting (See “The MOAP Bit” on page 44).

Knowing the system power state prior to a switch interrupt is required for correct Switch Event interpretation. The power state is defined by the following conditions:

V_{DD} present implies Power On

V_{CCH} present and V_{DD} absent implies Power Off.

If V_{BAT} falls below 2V with V_{CCH} absent, the oscillator, the timekeeping functions and the APC, all stop functioning.

If no external or battery-backup power is available, the system enters a No Power state. Upon leaving this state, the system is initialized.

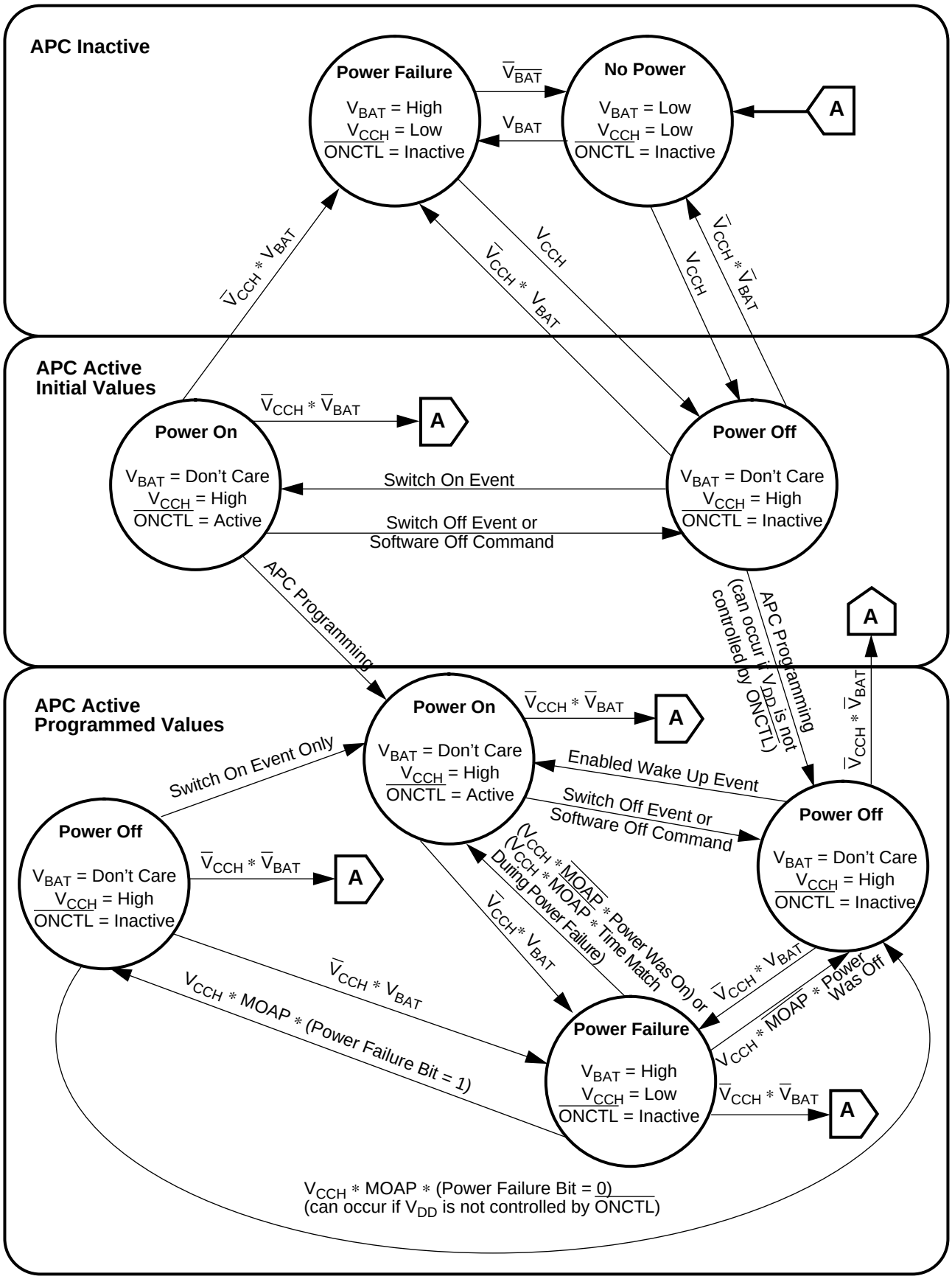


FIGURE 4-9. APC State Diagram

4.4 DETAILED FUNCTIONAL DESCRIPTION

4.4.1 The $\overline{\text{ONCTL}}$ Signal

The APC checks when activation or deactivation conditions are met, and sets or resets the $\overline{\text{ONCTL}}$ signal accordingly. This signal activates the system power supply. $\overline{\text{ONCTL}}$ is physically generated as the output of the $\overline{\text{ONCTL}}$ (set-reset) flip-flop. The state of $\overline{\text{ONCTL}}$ depends on the following:

- The status of the Mask $\overline{\text{ONCTL}}$ Activation (MOAP) bit
- Presence of activation conditions
- Power source condition
- The preceding state of $\overline{\text{ONCTL}}$

The Preceding State of the $\overline{\text{ONCTL}}$ Signal

A power failure may occur when the system is active or inactive. The $\overline{\text{ONCTL}}$ flip-flop maintains the state of the $\overline{\text{ONCTL}}$ signal at the time of the power failure. When power is restored, the $\overline{\text{ONCTL}}$ signal returns the system to a state determined by the saved status of $\overline{\text{ONCTL}}$ and the saved value of the MOAP bit.

The MOAP Bit

The Mask $\overline{\text{ONCTL}}$ Activation in Power Failure (MOAP) bit (bit 4 of APCR1) is controlled by software. It makes if possible to choose the desired system response upon return from a power failure, and decide whether the system remains inactive until it is manually switched on, or resumes the state that prevailed at the time of the power failure, including enabling of “wake-up” events, as described in the next section.

Logical Conditions that Define the Status of the $\overline{\text{ONCTL}}$ Flip-Flop

The logical conditions described here set or reset the $\overline{\text{ONCTL}}$ flip-flop. They reflect the physical events described in “System Power-Up and Power-Off Activation Event Description” on page 45.

Conditions that set the $\overline{\text{ONCTL}}$ flip-flop:

- Timer Enable bit is 1 and there is a match between the real-time clock and the time specified in the predetermined date registers.
- Switch On event occurred.
- Timer Match Enable bit is 1 and there is a match between the real-time clock and the time specified in the pre-determined date registers.

  User software must ensure unused date/time fields are coherent, to ensure the comparison of valid bits gives the correct results.
- The RING enable bit (bit 3 of APCR2) is 1 and one of the following occurs:
  - Bit 2 of APCR2 is 0, and a high-to-low transition is detected on the $\overline{\text{RING}}$ input pin.
  - Bit 2 0f APCR2 is 1 and a train of pulses is detected on the $\overline{\text{RING}}$ input pin.
- RI1,2 Enable bit(s) are 1 and a high to low transition is detected on the RI1,2 input pin(s).

Conditions that put the $\overline{\text{ONCTL}}$ flip-flop in a 1 state (inactive $\overline{\text{ONCTL}}$ signal):

- Switch Off Delay Enable bit is 0 and Switch Off event occurred.
- Switch Off Delay Enable bit is 1 and Fail-safe Timer reached terminal count.
- A 1 is written to Software Off Command bit.

4.4.2 Entering Power States

Power Up

When power is first applied to the RTC, the APC registers are initialized to default values defined in APCR1, APCR2 and APSR. See “Bank 2 Registers, APC Memory Bank” on page 51. This situation is defined by the appearance of V_{BAT} or V_{CCH} with no previous power.

The APC powers up when the RTC supply is applied from any source and is always in an active state. The RTC may be powered up, but inactive; this occurs if bit 0 of the register at index 30h (see Section 2.3 on page 13) of this logical device is not set. In this situation, the APC registers are not accessible, since they are only accessed via the RTC. This is also true of the general-purpose battery-backed RAM.

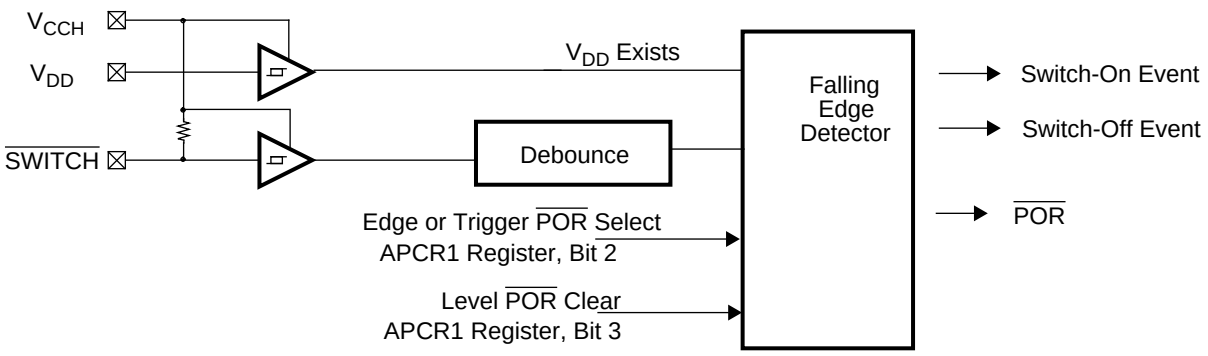


FIGURE 4-10. Switch Event Detector

Power Off Request ($\overline{POR}$)

The APC allows a maskable or non-maskable interrupt on the $\overline{POR}$ pin when the Switch Off event is detected on the $\overline{SWITCH}$ input pin.

This interrupt enables the user to perform an orderly exit procedure, automatically performing housekeeping functions such as file backups, printout completion and communications terminations, before powering down.

See Figure 4-10.

Power Failure

The APC is in a Power Failure state when it is powered by V_{BAT}, without V_{CCH}.

Upon entering a Power Failure state, the following events occur:

- The UART input signals ($\overline{RI2,1}$), the $\overline{SWITCH}$ (ON/OFF switch) pin and $\overline{RING}$ pin (for detecting telephone line incoming signals for fax, modem or voice communications) are masked (high).

  These signals remain masked until one second after exit from the Power Failure state, i.e., one second after switching from V_{BAT} to V_{CCH}, unless the MOAP bit is set to 1. See description of this bit on page 46.

- The $\overline{ONCTL}$ pin state is internally saved, and $\overline{ONCTL}$ is forced inactive.

  One second after power returns, the $\overline{ONCTL}$ signal reverts to its saved state, if the MOAP bit (Mask $\overline{ONCTL}$ Activation, i.e., bit 4) of the APCR1 register is cleared to 0. If the MOAP bit is set to 1, $\overline{ONCTL}$ remains inactive. If MOAP = 0, when the one second delay expires, new events can activate $\overline{ONCTL}$, unless a time match occurs during Power Failure, in which case the APC "remembers" to activate $\overline{ONCTL}$ at the end of the one second delay.

  If the MOAP bit (bit 4 of APCR1) and the Power Failure bit (bit 7 of APCR1) are both 1, then only the Switch On event can activate $\overline{ONCTL}$.

4.4.3 System Power-Up and Power-Off Activation Event Description

The APC may activate the host power supply when the following events occur:

- Physical On/Off switch is depressed and V_{DD} is absent.
- Preprogrammed wake-up time arrives.
- Communications input is detected on a modem.
- Ring signal is detected at a telephone input jack.

The PC may be powered down by the following events:

- Physical On/Off switch is depressed, and V_{DD} is present.
- Software controlled power down.
- Fail-safe power down in the event of power-down software hang-up. (See "Switch-Off Event".)

The $\overline{SWITCH}$ Input Signal

This signal provides two events: Switch-On and Switch-Off. In both, the physical switch line is debounced, i.e., the signal state is transferred only after 14 to 16 msec without transitions, which ensures the switch is no longer bouncing. See Figure 4-10.

Switch-On Event - Detection of a high to low transition on the debounced $\overline{SWITCH}$ input pin, when V_{DD} does not exist. The Switch-On event is masked (not detected) for one to two seconds after V_{DD} is removed.

Switch-Off Event - Detection of a high to low transition on the debounced $\overline{SWITCH}$ input pin, when V_{DD} exists. The Switch-Off event is masked for one to two seconds after V_{DD} was removed for the last time.

The Switch-Off event sets the Switch-Off Event Detect bit (bit 5 in APSR) to 1.

Switch-Off Delay - When the Switch Off Delay Enable bit (bit 6 in register APCR2) is 0, the Switch-Off event powers the system off immediately, i.e., the $\overline{ONCTL}$ output pin is deactivated immediately.

When the Switch-Off Delay Enable bit is 1 and a Switch-Off event occurs, a fail-safe timer starts a countdown of 5 or 21 seconds. (See bit 1 of the APCR1 register on page 46). If it is allowed to complete this sequence, the fail-safe timer sets the $\overline{ONCTL}$ signal high (inactive).

Switch-Off Event detection activates the Power-Off Request ($\overline{POR}$) that triggers a user-defined interrupt routine to conduct housekeeping activities prior to powering down. (The user may also detect the Switch-Off Event by polling the Switch-Off Detect bit, rather than the interrupt routine). The user must ensure that the power-off routine does not exceed the 5 or 21 second Switch-Off Delay, or else the routine must set bit 6 of APCR1 to stop and reset the fail-safe timer, thus preventing fail-safe timer causing power off before completion.

If the power-off routine gets "hung up", and the timer was not stopped and reset, then after the delay time has elapsed the timer will conclude its countdown and activate power off (deactivate $\overline{ONCTL}$).

The fails-safe timer is reset and stopped by writing 1 to the Fail-safe Timer Reset bit (bit 6 of APCR1). Switch-Off events detected while the timer is already counting are ignored. If during the count of the Fail-safe timer due to a switch off event with delay, VDD goes down, the fail safe timer is stopped and reset and $\overline{ONCTL}$ is not deactivated.

$\overline{POR}$ is asserted on a Switch-Off Event. It can be configured as either edge or level triggered, according to the APCR1 register, bit 2. In edge mode, it is a negative pulse, and in level mode it remains asserted until cleared by a level $\overline{POR}$ Clear Command (bit 3 of the APCR1 register, see Figure 4-10). Selection of $\overline{POR}$ on the GPIO22/$\overline{POR}$ pin is via the SuperI/O Configuration 2 register (at index 22h). Selection of the $\overline{POR}$ output buffer is via GPIO22 output buffer control bits (Port 2 Output Type and Port 2 Pull-up Control registers). See Table 8-1 on page 156.

Predetermined Wake-Up

The second, minute and hour values of the pre-determined wake-up times are contained in the Seconds Alarm, Minutes Alarm and Hours Alarm registers, respectively (indexes 01h, 03h and 05h of banks 0, 1 and 2). The Day of Week, Date of Month, Month, Year and Century of the pre-determined date is held in bank 2, registers indexes 43h-46h and 48h. These eight registers are compared with the corresponding Seconds, Minutes, Hours, Date of Week, Day of Month, Month and Year in all banks, register indexes 00, 02, 04, 06, 07, 08, 09 and Century register in bank 1, register index 48h.

Ring Signal Event

An incoming telephone call is an event that may activate a transfer from the Power-Off state to a Power-On state, in order to deal with the pending incoming voice, fax or modem communication.

The PC87308VUL can detect a $\overline{\text{RING}}$ pulse falling edge or a $\overline{\text{RING}}$ pulse train with a frequency of at least 16 Hz, that lasts at least 0.19 seconds.

During $\overline{\text{RING}}$ pulse train detection, the existence of falling edges on $\overline{\text{RING}}$ is monitored during time slots of 62.5 msec (16 Hz cycle time). A $\overline{\text{RING}}$ pulse train detect event occurs if falling edge(s) of $\overline{\text{RING}}$ were detected in three consecutive time slots, following a time slot in which no falling edge of $\overline{\text{RING}}$ was detected.

This method of detecting a $\overline{\text{RING}}$ pulse train filters out (does not detect) a $\overline{\text{RING}}$ pulse train of less then 11 Hz, might detect a $\overline{\text{RING}}$ pulse train of 11 Hz to 16 Hz, and guarantees detection of a $\overline{\text{RING}}$ pulse train of at least 16 Hz.

$\overline{\text{RI1,2}}$ Event

High to Low transitions on $\overline{\text{RI1}}$ or $\overline{\text{RI2}}$ indicate communications activity on the UART inputs, and these conditions may be used as events to “wake-up” the system.

NOTE: The APC can distinguish between two events of the same type if a minimum time of 2.5 periods of the 32Khz clock passed between their arivals. Thus, if the APC detects an event, and another event of the same nature occurs once again in less than 70ms from the previous event, the APC might not detect the second event ,i.e., the event will be lost.

4.5 APC REGISTERS

The APC registers reside in the APC bank 2 memory. The RAM Lock register also resides in this bank. See Table 4-4 on page 41.

The APC registers are not affected by system reset. They are initialized to 0 only when power is applied for the first time, i.e., application of one of the voltages V_{BAT} or V_{CCH} when no previous voltage was present.

4.5.1 APC Control Register 1 (APCR1), Index 40h

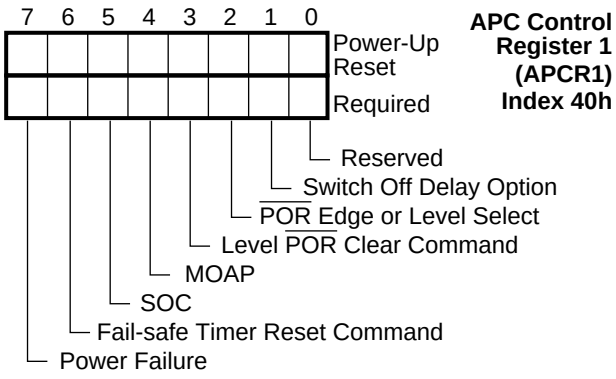


FIGURE 4-11. APCR1 Register Bitmap

Bit 0 - Reserved

Reserved.

Bit 1 - Switch Off Delay Option

0 - 4-5 seconds.

1 - 20-21 seconds.

Bit 2 - $\overline{\text{POR}}$ Edge or Level Select

0 - Edge $\overline{\text{POR}}$.

1 - Level $\overline{\text{POR}}$. Once $\overline{\text{POR}}$ is asserted, it remains asserted until cleared by Level $\overline{\text{POR}}$ Clear Command (bit 3).

Bit 3 - Level $\overline{\text{POR}}$ Clear Command

This is a write-only non-sticky bit. Read returns 0.

0 - Ignored.

1 - $\overline{\text{POR}}$ output signal is deactivated.

Bit 4 - Mask $\overline{\text{ONCTL}}$ Activation if Power Fail (MOAP)

0 - When power returns, sets the system to the power state that existed when power failed.

1 - While the Power Failure bit (bit 7 of APCR1) is set, mask $\overline{\text{ONCTL}}$ activation, except as a result of a Switch On Event.

Bit 5 - Software Off Command (SOC)

This bit is write-only and non-sticky. Read returns 0.

0 - Ignored.

1 - $\overline{\text{ONCTL}}$ output signal is deactivated.

Bit 6 - Fail-safe Timer Reset Command

This bit is write-only and non-sticky. Read returns 0.

0 - Ignored.

1 - Fail-safe timer is stopped and reset.

Bit 7 - Power Failure

Set to 1 when RTC/APC switches from V_{CCH} to V_{BAT}. Cleared to 0 by writing 1 to this bit. Writing 0 to this bit has no effect.

4.5.2 APC Control Register 2 (APCR2), Index 41h

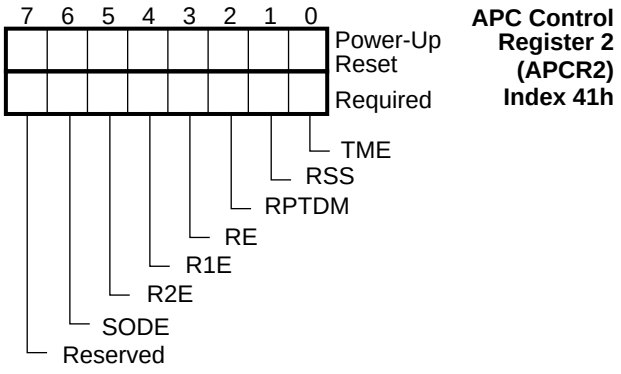


FIGURE 4-12. APCR2 Register Bitmap

Bit 0 - Timer Match Enable (TME)

0 - Pre-determined date or time event is ignored.

1 - Match between the RTC and the pre-determined date and time activates the $\overline{\text{ONCTL}}$ output signal.

See MOAP (bit 4) of APCR1 for an overriding case.

Bit 1 - $\overline{\text{RING}}$ Source Select (RSS)

0 - $\overline{\text{RING}}$ source is $\overline{\text{RING}}/\overline{\text{XDCS}}$ signal, regardless of X-bus Data Buffer (XDB) select bit of SuperI/O Configuration 1 register.

1 - $\overline{\text{RING}}$ source is GPIO23/$\overline{\text{RING}}$ signal.

Bit 2 - $\overline{\text{RING}}$ Pulse or Train Detection Mode (RPTDM)

0 - Detection of $\overline{\text{RING}}$ pulse falling edge.

1 - Detection of $\overline{\text{RING}}$ pulse train above 16 Hz for 0.19 sec.

Bit 3 - $\overline{\text{RING}}$ Enable (RE)

0 - $\overline{\text{RING}}$ input signal is ignored.

1 - $\overline{\text{RING}}$ detection activates the $\overline{\text{ONCTL}}$ output signal, unless it is overridden by the MOAP bit, bit 4 of the APCR1 register.

Bit 4 - $\overline{\text{RI1}}$ Enable (R1E)

0 - $\overline{\text{RI1}}$ input signal is ignored.

1 - A high to low transition on the $\overline{\text{RI1}}$ input pin activates the $\overline{\text{ONCTL}}$ output pin.

See MOAP (bit 4) of APCR1 for an overriding case.

Bit 5 - $\overline{\text{RI2}}$ Enable (R2E)

0 - $\overline{\text{RI2}}$ input signal is ignored.

1 - A high to low transition on the $\overline{\text{RI2}}$ input pin activates the $\overline{\text{ONCTL}}$ output pin.

See MOAP (bit 4) of APCR1 for an overriding case.

Bit 6 - Switch Off Delay Enable (SODE)

0 - $\overline{\text{ONCTL}}$ output pin is deactivated immediately after the Switch Off event.

1 - After the Switch Off Event, $\overline{\text{ONCTL}}$ output signal is deactivated after a 5 or 21 second Switch Off delay.

Bit 7 - Reserved

This bit is reserved.

4.5.3 APC Status Register (APSR), Index 42h

Bits 5-0 in this register are cleared to 0, when this register is read.

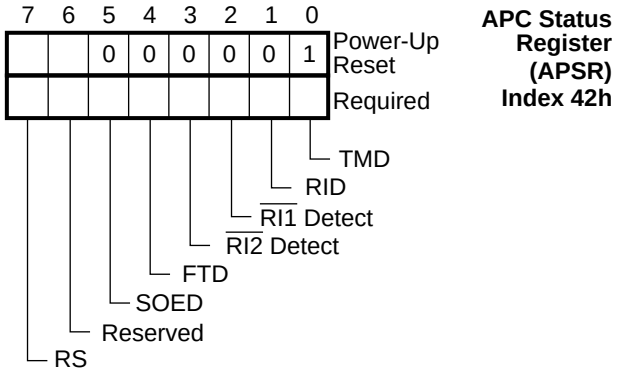


FIGURE 4-13. APSR Register Bitmap

Bit 0 - Timer Match Detect (TMD)

This bit is set to 1 when the RTC reaches the pre-determined date, regardless of the Timer Match Enable bit (bit 0 of APCR2). After first Power-Up, the RTC and the pre-determined date, are 0 and so this bit is set. It is recommended to clear this bit by reading this register after first Power-Up.

Bit 1 - $\overline{\text{RING}}$ Detect (RID)

This bit is set to 1 when a high to low transition is detected on the $\overline{\text{RING}}$ input pin and bit 2 of APCR2 is 0, or when a $\overline{\text{RING}}$ pulse train is detected on the $\overline{\text{RING}}$ input pin and bit 2 of APCR2 is 1, regardless of the status of the $\overline{\text{RING}}$ enable bit.

Bit 2 - $\overline{\text{RI1}}$ Detect

This bit is set to 1 when a high to low transition is detected on the $\overline{\text{RI1}}$ input signal, regardless of the $\overline{\text{RI1}}$ Enable bit.

Bit 3 - $\overline{\text{RI2}}$ Detect.

This bit is set to 1 when a high to low transition is detected on the $\overline{\text{RI2}}$ input pin, regardless of the $\overline{\text{RI2}}$ Enable bit.

Bit 4 - Fail-Safe Timer Detect (FTD)

This bit is set to 1 when the Fail-safe timer reaches terminal count.

Bit 5 - Switch Off Event Detect (SOED)

This bit is set to 1 when a Switch Off event is detected, regardless of the Switch Off Delay Enable bit.

Bit 6 - Reserved

Reserved.

Bit 7 - $\overline{\text{RING}}$ Status Bit (RS)

Holds the instantaneous value of the selected $\overline{\text{RING}}$ pin.

4.5.4 RAM Lock Register (RLR), Index 47h

Once a non-reserved bit is set to 1 it can be cleared only by hardware (MR pin) reset.

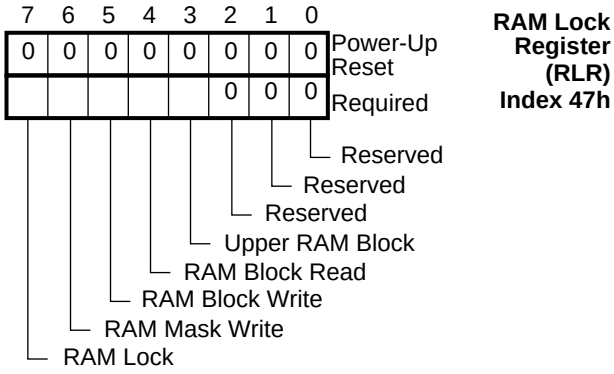


FIGURE 4-14. RAM Lock Register

Bit 2-0 - Reserved

Reserved.

Bit 3 - Upper RAM Block

Controls access to the upper 128 RAM bytes, accessed via the Upper RAM Address and Data Ports of bank 1

0 - This bit has no effect on upper RAM access.

1 - Upper RAM Data Port of bank 1 is blocked: writes are ignored and reads return FFh.

Bit 4 - RAM Block Read

This bit controls reads from RAM bytes 80h-9Fh (00h-1Fh of upper RAM).

0 - This bit has no effect on upper RAM access.

1 - Reads from bytes 00h-1Fh of upper RAM return FFh.

Bit 5 - RAM Block Write

This bit controls writes to bytes 80h-9Fh (00h-1Fh of upper RAM).

0 - This bit has no effect on upper RAM access.

1 - Writes to bytes 00h-1Fh of upper RAM are ignored.

Bit 6 - RAM Mask Write

This bit controls writes to all RTC RAM.

0 - This bit has no effect on RAM access.

1 - Writes to bank 0 RAM and to upper RAM are ignored.

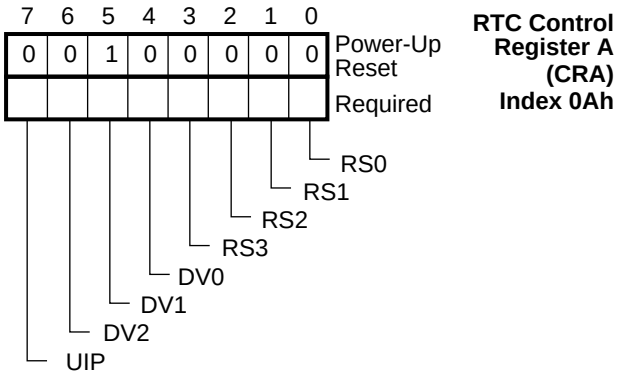
Bit 7 - RAM Lock

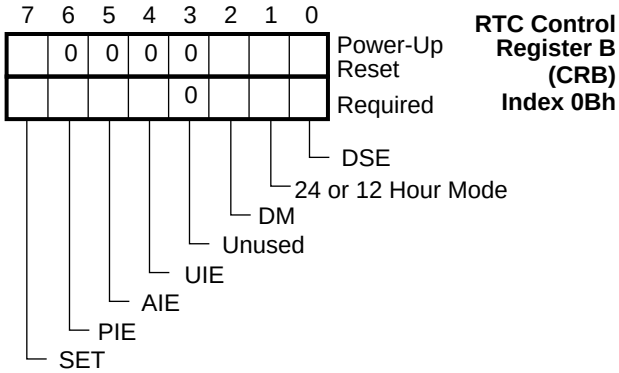
0 - This bit has no effect on RAM access.

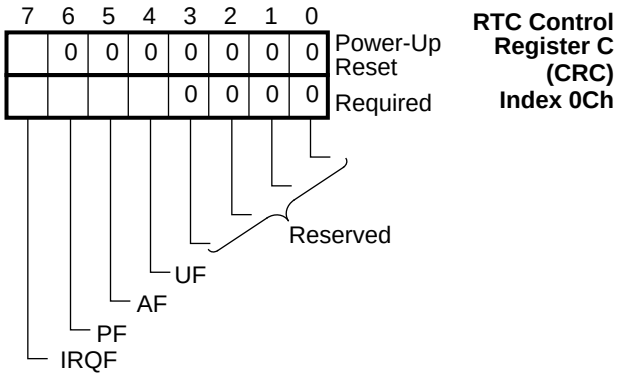
1 - Read and write to locations 38h-3Fh of all banks are blocked. Writes are ignored, and reads return FFh.

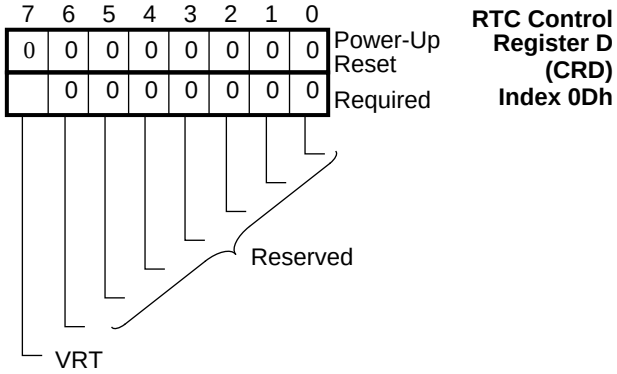
4.6 RTC AND APC REGISTER BITMAPS

4.6.1 RTC Register Bitmaps

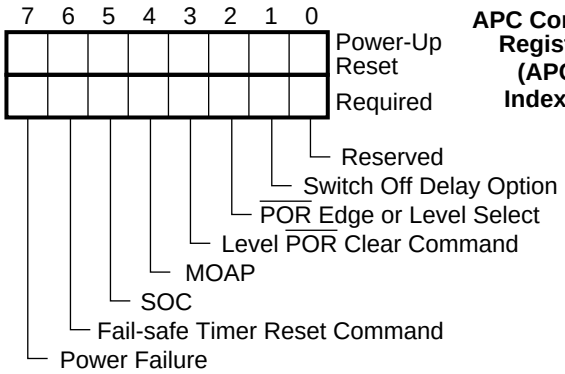




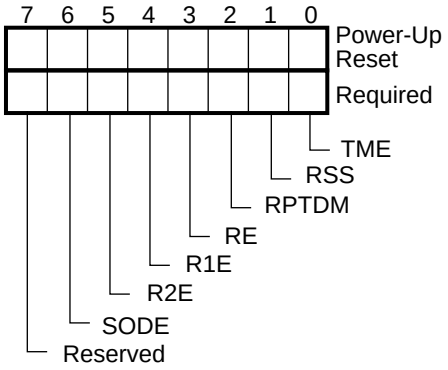




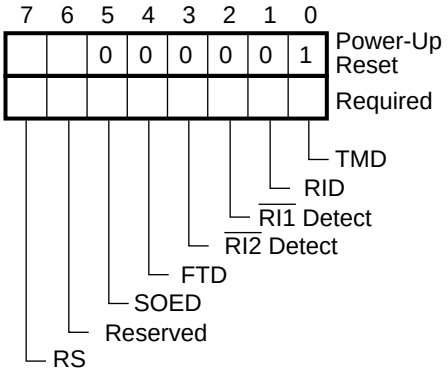
4.6.2 APC Register Bitmaps



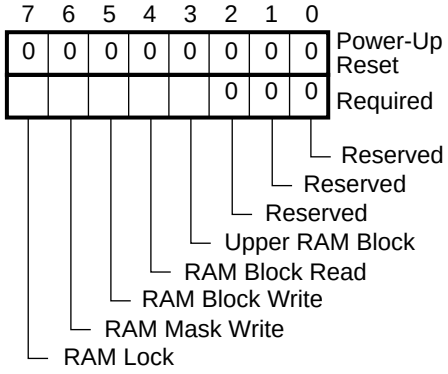
APC Control Register 1 (APCR1) Index 40h



APC Control Register 2 (APCR2) Index 41h



APC Status Register (APSR) Index 42h



RAM Lock Register (RLR) Index 47h

4.7 REGISTER BANK TABLES

TABLE 4-6. Banks 1 and 2, Common 64-Byte Memory Map

Index	Function	BCD Format	Binary Format	Comments
00h	Seconds	00-59	00-3b	R/W
01h	Seconds Alarm	00-59	00-3b	R/W
02h	Minutes	00-59	00-3b	R/W
03h	Minutes Alarm	00-59	00-3b	R/W
04h	Hours	12 hr = 01-12 (AM)	01-0c (AM)	R/W
		12 hr = 81-92 (PM)	81-8c (PM)	R/W
		24 hr = 00-23	00-17	R/W
05h	Hours Alarm	12 hr = 01-12 (AM)	01-0c (AM)	R/W
		12 hr = 81-92 (PM)	81-8c (PM)	R/W
		24 hr = 00-23	00-17	R/W
06h	Day of Week	01-07	01-07 (Sunday = 1)	R/W
07h	Date of Month	01-31	01-1f	R/W
08h	Month	01-12	01-0c	R/W
09h	Year	00-99	00-63	R/W
0Ah	Control Register A			R/W (bit 7 is read only)
0Bh	Control Register B			R/W (bit 3 is read only)
0Ch	Control Register C			All bits read only
0Dh	Control Register D			All bits read only
0Eh-3Fh	General Purpose RAM			R/W

TABLE 4-7. Bank 0 Registers, General Purpose Memory Bank

Register	Index	Type	Power-on Value	Function
	00h-3Fh			The first 14 RTC registers and the first 50 RTC RAM bytes are shared among banks 0, 1 and 2.
	40h - 7Fh	R/W		General Purpose 64-Byte Battery-Backed RAM.

TABLE 4-8. Bank 1 Registers, RTC Memory Bank

Register	Index	Type	Power-on Value	Function
	00h-3Fh			Banks 0, 1 and 2 share the first 14 RTC registers and the first 50 RTC RAM bytes.
	40h-47h			Reserved. Writes have no effect and reads return 00h
Century	48h	R/W	00h	BCD Format: 00-99. Binary Format: 00-63
	49h-4Fh			Reserved
Upper RAM Address Port	50h	R/W		Bits 6-0: Address of the upper 128 RAM bytes. Bit 7: Reserved.
	51h-52h			Reserved
Upper RAM Data Port	53h	R/W		The byte pointed by the Upper RAM Address Port is accessed via this register.
	54h-7Fh			Reserved

TABLE 4-9. Bank 2 Registers, APC Memory Bank

Register	Index	Type	Power-On Value	Function
	00h - 3Fh			Banks 0, 1 and 2 share the first 14 RTC registers and the first 50 bytes of RTC RAM.
APC Control Register 1 (APCR1)	40h	R/W	00h	See “APC Control Register 1 (APCR1), Index 40h” on page 46
APC Control Register 2 (APCR2)	41h	R/W	00h	See “APC Control Register 2 (APCR2), Index 41h” on page 47
APC Status Register (APSR)	42h	R	1000001 (binary) (bit 7 is indeterminate)	See “APC Status Register (APSR), Index 42h” on page 47
Wake Up Day of Week	43h	R/W		BCD Format: 01-07 Binary Format: 01-07 (Sunday = 1)
Wake Up Date of Month	44h	R/W		BCD Format: 01-31 Binary Format: 01-1F
Wake Up Month	45h	R/W		BCD Format: 01-12 Binary Format: 01-0C
Wake Up Year	46h	R/W		BCD Format: 00-99 Binary Format: 00-63
RAM Lock	47h	R/W	00h; initialized also on MR pin reset.	See “RAM Lock Register (RLR), Index 47h” on page 48
Wake Up Century	48h	R/W		BCD Format: 00-99 Binary Format: 00-63
	49h-7Fh			Reserved

TABLE 4-10. Available General Purpose Bytes

Index	Bank	Number of Bytes	Notes
0Eh - 3Fh	All	50	
40h - 7Fh	Bank 0	64	
50h, 53h	Bank 1	128	Indirect access via 50h for address and 53h for data.
Total		**242**	

5.0 The Floppy Disk Controller (FDC) (Logical Device 3)

5.1 FDC FUNCTIONAL DESCRIPTION

The PC87308VUL is software compatible with the DP8473 and 82077 floppy disk controllers. Upon a power on reset, the 16-byte FIFO will be disabled. Also, the disk interface outputs will be configured as active push-pull outputs, which are compatible with both CMOS inputs and open-collector resistor terminated disk drive inputs. The FIFO can be enabled with the Configure command. The FIFO can be very useful at the higher data rates, with systems that have a large amount of DMA bus latency, or with multi-tasking systems such as the EISA or MCA bus structures.

The FDC will support all the DP8473 Mode command features as well as some additional features. These include control over the enabling of the FIFO for reads and writes, a Non-Burst mode for the FIFO, a bit that will configure the disk interface outputs as open-drain outputs, and programmability of the DENSEL output.

5.1.1 Microprocessor Interface

The FDC interface to the microprocessor consists of the A15 - A3, AEN, $\overline{RD}$, and $\overline{WR}$ lines, which access the chip for reads and writes; the data lines D7-D0; the address lines A2-A0, which select the appropriate register (see Table 5-1); the IRQ signal, and the DMA interface signals DRQ, $\overline{DACK}$, and TC. It is through this microprocessor interface that the floppy controller receives commands, transfers data, and returns status information.

5.1.2 Modes of Operation

The FDC has two modes of operation: PC-AT mode and PS/2 mode, which are determined by the state of bit 6 of of the SuperI/O FDC Configuration register (at index 0xF0) as described in Section 2.6.1 on page 23. See “FDC Register Description” on page 59 for more details on the register set used for each mode of operation.

PC-AT mode - Bit 6 of of the SuperI/O FDC Configuration register (at index 0xF0) is 0 (default): the PC-AT register set is enabled. The DMA enable bit in the Digital Output Register becomes valid (IRQ and DRQ can be TRI-STATE). TC and DENSEL become active high signals (defaults to a 5.25" floppy drive).

PS/2 mode - Bit 6 of of the SuperI/O FDC Configuration register (at index 0xF0) is 1: this mode supports the PS/2 Models 50/60/80 configuration and register set. The DMA enable bit in the Digital Output Register becomes a don't care (IRQ and DRQ signals are always valid). TC and DENSEL become active low signals (default to 3.5" floppy drive).

5.1.3 Controller Phases

The FDC has three separate phases of a command, the Command Phase, the Execution Phase, and the Result Phase. Each of these controller phases determine how data is transferred between the floppy controller and the host microprocessor. In addition, when no command is in progress, the controller is in the Idle Phase or Drive Polling Phase.

Command Phase

During the Command Phase, the µP writes a series of bytes to the Data Register. The first command byte contains the opcode for the command, and the controller knows how many more bytes to expect based on this opcode byte. The remaining command bytes contain the particular parameters required for the command. The number of command bytes varies for each particular command. All the command bytes must be written in the order specified in the Command Description Table. The Execution Phase starts immediately after the last byte in the Command Phase is written. Prior to performing the Command Phase, the Digital Output Register should be set and the data rate should be set with the Data Rate Select Register or Configuration Control Register.

The Main Status Register controls the flow of command bytes, and must be polled by the software before writing each Command Phase byte to the Data Register. Prior to writing a command byte, the RQM bit (D7) must be set and the DIO bit (D6) must be cleared in the MSR. After the first command byte is written to the Data Register, the CMD PROG bit (D4) is also set and remains set until the last Result Phase byte is read. If there is no Result Phase, the CMD PROG bit is cleared after the last command byte is written.

A new command may be initiated after reading all the result bytes from the previous command. If the next command requires selecting a different drive or changing the data rate, the DOR and DSR or CCR should be updated. If the command is the last command, the software should deselect the drive.

Note:

As a general rule, the operation of the controller core is independent of how the µP updates the DOR, DSR, and CCR. The software must ensure that the manipulation of these registers is coordinated with the controller operation.

Execution Phase

During the Execution Phase, the disk controller performs the desired command. Commands that involve data transfers (e.g., read, write, or format operation) require the µP to write or read data to or from the Data Register at this time. Some commands such as a Seek or Recalibrate control the read/write head movement on the disk drive during the Execution Phase via the disk interface signals. Execution of other commands does not involve any action by the µP or disk drive, and consists of an internal operation by the controller.

If there is data to be transferred between the µP and the controller during the Execution, there are three methods that can be used, DMA mode, interrupt transfer mode, and software polling mode. The last two modes are called the Non-DMA modes. The DMA mode is used if the system has a DMA controller. This allows the µP to do other tasks while the data transfer takes place during the Execution Phase. If the Non-DMA mode is used, an interrupt is issued for each byte transferred during the Execution Phase. Also, instead of using the interrupt during Non-DMA mode, the Main Status Register can be polled by software to indicate when a byte transfer is required. All of these data transfer modes work with the FIFO enabled or disabled.

DMA Mode - FIFO Disabled

The DMA mode is selected by writing a 0 to the DMA bit in the Specify command and by setting the DMA enabled bit (D3) in the DOR. With the FIFO disabled, a DMA request (DRQ) is generated in the Execution Phase when each byte is ready to be transferred. The DMA controller should respond to the DRQ with a DMA acknowledge ($\overline{DACK}$) and a read or write strobe. The DRQ is cleared by the leading edge

of the active low $\overline{DACK}$ input signal. After the last byte is transferred, an interrupt is generated, indicating the beginning of the Result Phase. During DMA operations the address signals are ignored since AEN input signal is 1. The DACK signal acts as the chip select for the FIFO in this case, and the state of the address lines A2-0 doesn't matter. The Terminal Count (TC) signal can be asserted by the DMA controller to terminate the data transfer at any time. Due to internal gating, TC is only recognized when $\overline{DACK}$ is low.

PC-AT mode. When in the PC-AT interface mode with the FIFO disabled, the controller is in single byte transfer mode. That is, the system has one byte time to service a DMA request (DRQ) from the controller. DRQ is deasserted between each byte.

PS/2 mode. When in the PS/2 mode, DMA transfers with the FIFO disabled are performed differently. Instead of a single byte transfer mode, the FIFO is actually enabled with THRESH = 0Fh. Thus, DRQ is asserted when one byte has entered the FIFO during reads, and when one byte can be written to the FIFO during writes. DRQ is deasserted by the leading edge of the $\overline{DACK}$ input, and is reasserted when DACK goes inactive high. This operation is very similar to Burst mode transfer with the FIFO enabled except that DRQ is deasserted between each byte.

DMA Mode - FIFO Enabled

Read Data Transfers Whenever the number of bytes in the FIFO is greater than or equal to (16 - THRESH), a DRQ is generated. This is the trigger condition for the FIFO read data transfers from the floppy controller to the µP.

Burst Mode. DRQ remains active until enough bytes have been read from the controller to empty the FIFO.

Non-Burst Mode. DRQ is deasserted after each read transfer. If the FIFO is not completely empty, DRQ is reasserted after a 350 ns delay. This allows other higher priority DMA transfers to take place between floppy transfers. In addition, this mode allows the controller to work correctly in systems where the DMA controller is put into a read verify mode, where only $\overline{DACK}$ signals are sent to the FDC, with no $\overline{RD}$ pulses. This read verify mode of the DMA controller is used in some PC software. The FIFO Non-Burst mode allows the $\overline{DACK}$ input from the DMA controller to be strobed, which correctly clocks data from the FIFO.

For both the Burst and Non-Burst modes, when the last byte in the FIFO has been read, DRQ goes inactive. DRQ is then be reasserted when the FIFO trigger condition is satisfied. After the last byte of a sector has been read from the disk, DRQ is again generated even if the FIFO has not yet reached its threshold trigger condition. This guarantees that all the current sector bytes are read from the FIFO before the next sector byte transfer begins.

Write Data Transfers Whenever the number of bytes in the FIFO is less than or equal to THRESH, a DRQ is generated. This is the trigger condition for the FIFO write data transfers from the µP to the floppy controller.

Burst Mode. DRQ remains active until enough bytes have been written to the controller to completely fill the FIFO.

Non-Burst Mode. DRQ is deasserted after each write transfer. If the FIFO is not full, DRQ is reasserted after a 350 ns delay. This deassertion of DRQ allows other higher priority DMA transfers to take place between floppy transfers.

The FIFO has a byte counter which monitors the number of bytes being transferred to the FIFO during write operations for both Burst and Non-Burst modes. When the last byte of a sector is transferred to the FIFO, DRQ is deasserted even if the FIFO has not been completely filled. Thus, the FIFO is cleared after each sector is written. Only after the floppy controller has determined that another sector is to be written is DRQ asserted again. Also, since DRQ is deasserted immediately after the last byte of a sector is written to the FIFO, the system does not need to tolerate any DRQ deassertion delay and is free to do other work.

Read and Write Data Transfers The $\overline{DACK}$ input signal from the DMA controller may be held active during an entire burst or it may be strobed for each byte transferred during a read or write operation. When in the Burst mode, the floppy controller deasserts DRQ as soon as it recognizes that the last byte of a burst was transferred. If $\overline{DACK}$ is strobed for each byte, the leading edge of this strobe is used to deassert DRQ. If DACK is strobed $\overline{RD}$ or $\overline{WR}$ are not required. This is the case during the Read-Verify mode of the DMA controller. If DACK is held active during the entire burst, the trailing edge of the $\overline{RD}$ or $\overline{WR}$ strobe is used to deassert DRQ. DRQ is deasserted within 50 ns of the leading edge of $\overline{DACK}$, $\overline{RD}$, or $\overline{WR}$. This quick response should prevent the DMA controller from transferring extra bytes in most applications.

Overrun Errors An overrun or underrun error terminates the execution of the command if the system does not transfer data within the allotted data transfer time (see Section 5.2.7 on page 64), which puts the controller into the Result Phase. During a read overrun, the µP is required to read the remaining bytes of the sector before the controller asserts IRQ, signifying the end of execution. During a write operation, an underrun error terminates the Execution Phase after the controller has written the remaining bytes of the sector with the last correctly written byte to the FIFO and generated the CRC bytes. Whether there is an error or not, an interrupt is generated at the end of the Execution Phase, and is cleared by reading the first Result Phase byte.

DACK asserted alone without a RD or WR strobe is also counted as a transfer. If RD or WR are not being strobed for each byte, DACK must be strobed for each byte so that the floppy controller can count the number of bytes correctly. A new command, the Verify command, has been added to allow easier verification of data written to the disk without the need of actually transferring the data on the data bus.

Interrupt Mode - FIFO Disabled

If the Interrupt (Non-DMA) mode is selected, IRQ is asserted instead of DRQ when each byte is ready to be transferred. The Main Status Register should be read to verify that the interrupt is for a data transfer. The RQM and Non-DMA bits (D7 and D5) in the MSR are set. The interrupt is cleared when the byte is transferred to or from the Data register. To transfer the data in or out of the Data register, you must use the address bits of the FDC together and $\overline{RD}$ or $\overline{WR}$ must be active, i.e., A2-0 must be valid. It is not enough to just assert the address bits of the FDC. $\overline{RD}$ or $\overline{WR}$ must also be active for a read or write transfer to be recognized.

The µP should transfer the byte within the data transfer service time (see Section 5.2.7 on page 64). If the byte is not transferred within the time allotted, an Overrun Error is indicated in the Result Phase when the command terminates at the end of the current sector.

An interrupt is also generated after the last byte is transferred. This indicates the beginning of the Result Phase. The RQM and DIO bits (D7 and D6) in the MSR is set, and the NON DMA bit (D5) is cleared. This interrupt is cleared by reading the first result byte.

Interrupt Mode - FIFO Enabled

The Interrupt (Non-DMA) mode with the FIFO enabled is very similar to the Non-DMA mode with the FIFO disabled. In this case, IRQ is asserted instead of DRQ under the exact same FIFO threshold trigger conditions. The MSR should be read to verify that the interrupt is for a data transfer. The RQM and Non-DMA bits (D7 and D5) in the MSR is set. To transfer the data in or out of the Data register, you must use the address bits of the FDC together and $\overline{RD}$ or $\overline{WR}$ must be active, i.e., A2-0 must be valid. It is not enough to just assert the address bits of the FDC. $\overline{RD}$ or $\overline{WR}$ must also be active for a read or write transfer to be recognized.

The Burst mode may be used to hold the IRQ pin active during a burst, or the Non-Burst mode may be used to toggle the IRQ pin for each byte of a burst. The Main Status Register is always valid from the µP point of view. For example, during a read command, after the last byte of data has been read from the disk and placed in the FIFO, the MSR still indicates that the Execution Phase is active, and that data needs to be read from the Data Register. Only after the last byte of data has been read by the µP from the FIFO does the Result Phase begin.

The same overrun and underrun error procedures from the DMA mode apply to the Non-DMA mode. Also, whether there is an error or not, an interrupt is generated at the end of the Execution Phase, and is cleared by reading the first Result Phase byte.

Software Polling

If the Non-DMA mode is selected and interrupts are not suitable, the µP can poll the MSR during the Execution Phase to determine when a byte is ready to be transferred. The RQM bit (D7) in the MSR reflects the state of the IRQ signal. Otherwise, the data transfer is similar to the Interrupt Mode described above. This is true for the FIFO enabled or disabled.

Result Phase

During the Result Phase, the µP reads a series of bytes from the data register. These bytes indicate the status of the command. This status may indicate whether the command executed properly, or contain some control information (see the Command Description Table and Status Register Description). These Result Phase bytes are read in the order specified for that particular command. Some commands do not have a result phase. Also, the number of result bytes varies with each command. All of the result bytes must be read from the Data Register before the next command can be issued.

Like the Command Phase, the Main Status Register controls the flow of result bytes, and must be polled by the software before reading each Result Phase byte from the Data Register. The RQM bit (D7) and DIO bit (D6) must both be set before each result byte can be read. After the last result byte is read, the COM PROG bit (D4) in the MSR is cleared, and the controller is ready for the next command.

Idle Phase

After a hardware or software reset, or after the chip has recovered from the power down mode, the controller enters the Idle Phase. Also, when there are no commands in progress the controller is in the Idle Phase. The controller waits for a command byte to be written to the Data Register. The RQM bit is set and the DIO bit is cleared in the MSR. After receiving the first command (opcode) byte, the controller enters the Command Phase. When the command is completed the controller again enters the Idle Phase. The Data Separator remains synchronized to the reference frequency while the controller is idle. While in the Idle Phase, the controller periodically enters the Drive Polling Phase (see below).

Drive Polling Phase

The NSC FDC supports the polling mode of the old generation 8-inch drives as a means of monitoring any change in status for each disk drive present in the system. This mode is supported for the sole purpose of providing backward compatibility with software that expects its presence.

While in the Idle Phase the controller enters a Drive Polling Phase every 1 ms (based on the 500 Kbps data rate). While in the Drive Polling Phase, the controller interrogates the Ready Changed status for each of the four logical drives. The internal Ready line for each drive is toggled only after a hardware or software reset, and an interrupt is generated for drive 0. At this point, the software must issue four Sense Interrupt commands to clear the Ready Changed State status for each drive. This requirement can be eliminated if drive polling is disabled via the POLL bit in the Configure command. The Configure command must be issued within 500 us (worst case) of the hardware or software reset for drive polling to be disabled.

Even if drive polling is disabled, drive stepping and delayed power-down occur in the Drive Polling Phase. The controller checks the status of each drive and if necessary it issues a step pulse on the STEP output with the DIR signal at the appropriate logic level. Also, the controller uses the Drive Polling Phase to control the Automatic Low Power mode. When the Motor Off time has expired, the controller waits 512 ms based on the 500 Kbps and 1 Mbps data rate before powering down if this function is enabled via the Mode command.

If a new command is issued when the FDC is in the middle of a polling routine, the MSR will not indicate a ready status for the next parameter byte until the polling sequence completes the loop. This can cause a delay between the first and second bytes of up to 500 µs at 250 kbps.

5.1.4 Data Separator

The internal data separator consists of an analog PLL and its associated circuitry. The PLL synchronizes the raw data-signal read from the disk drive. The synchronized signal is used to separate the encoded clock and data pulses. The data pulses are deserialized into bytes and then sent to the µP by the controller.

The main PLL consists of five main components, a phase comparator, a charge pump, a filter, a voltage controlled oscillator (VCO), and a programmable divider. The phase comparator detects the difference between the phase of the divider's output and the phase of the raw data being read from the disk. This phase difference is converted to a current by the charge pump, which either charges or discharges one of three filters which is selected based on the data rate. The resulting voltage on the filter changes the frequency of the VCO and the divider output to reduce the phase difference between the input data and the divider's output. The PLL is “locked” when the frequency of the divider is ex-

actly the same as the average frequency of the data read from the disk. A block diagram of the data separator is shown in Figure 5-1.

To ensure optimal performance, the data separator incorporates several additional circuits. The quarter period delay line is used to determine the center of each bit cell, and to disable the phase comparator when the raw data signal is missing a clock or data pulse in the MFM or FM pattern. A secondary PLL is used to automatically calibrate the quarter period delay line. The secondary PLL also calibrates the center frequency of the VCO.

To eliminate the logic associated with controlling multiple data rates, the FDC supports each of the four data rates (250, 300, 500 Kbps, and 1 Mbps) with a separate, optimized internal filter. The appropriate filter for each data rate is automatically switched into the data separator circuit when the data rate is selected via the Data Rate Select or Configuration Control Register. These filters have been optimized through lab experimentation, and are designed into the controller to reduce the external component cost associated with the floppy controller.

The FDC has a dynamic window margin and lock range performance capable of handling a wide range of floppy disk drives. Also, the data separator works well under a variety of conditions, including the high motor speed fluctuations of floppy compatible tape drives.

Figure 5-2 shows the floppy disk controller dynamic window margin performance at the four different data rates. Dynamic window margin is the primary indicator of the quality and performance level of the data separator. This measurement indicates how much motor speed variation (MSV) of the drive spindle motor and bit jitter (or window margin) can be tolerated by the data separator.

MSV is shown on the x-axis of the dynamic window margin graph. MSV is translated directly to the actual data rate of the data as it is read from the disk by the data separator. That is, a faster than nominal motor results in a higher frequency in the actual data rate.

The dynamic window margin performance curves also indicate how much bit jitter (or window margin) can be tolerated by the data separator. This parameter is shown on the y-axis of the graphs. Bit jitter is caused by the magnetic interaction of adjacent data pulses on the disk, which effectively shifts the bits away from their nominal positions in the middle of the bit window. Window margin is commonly measured as a percentage. This percentage indicates how far a data bit can be shifted early or late with respect to its nominal bit position, and still be read correctly by the data separator. If the data separator cannot correctly decode a shifted bit, then the data is misread and a CRC results.

The dynamic window margin performance curves contain two pieces of information: 1) the maximum range of MSV (also called “lock range”) that the data separator can handle with no read errors, and 2) the maximum percentage of window margin (or bit jitter) that the data separator can handle with no read errors. Thus, the area under the dynamic window margin curves in Figure 5-2 is the range of MSV and bit jitter that the FDC can handle with no read errors. The FDC internal analog data separator has a much better performance than comparable digital data separator designs, and does not require any external components.

Note:

The dynamic window margin curves were generated using a FlexStar FS-540 Floppy Disk Simulator and a proprietary dynamic window margin test program written by National Semiconductor.

The controller takes best advantage of the internal analog data separator by implementing a sophisticated read algorithm. This ID search algorithm, shown in Figure 5-3, enhances the lock characteristics of the PLL by forcing the PLL to relock to the crystal reference frequency any time the data separator attempts to lock to a non-preamble pattern. This algorithm ensures that the PLL is not thrown way out of lock by write splices or bad data fields.

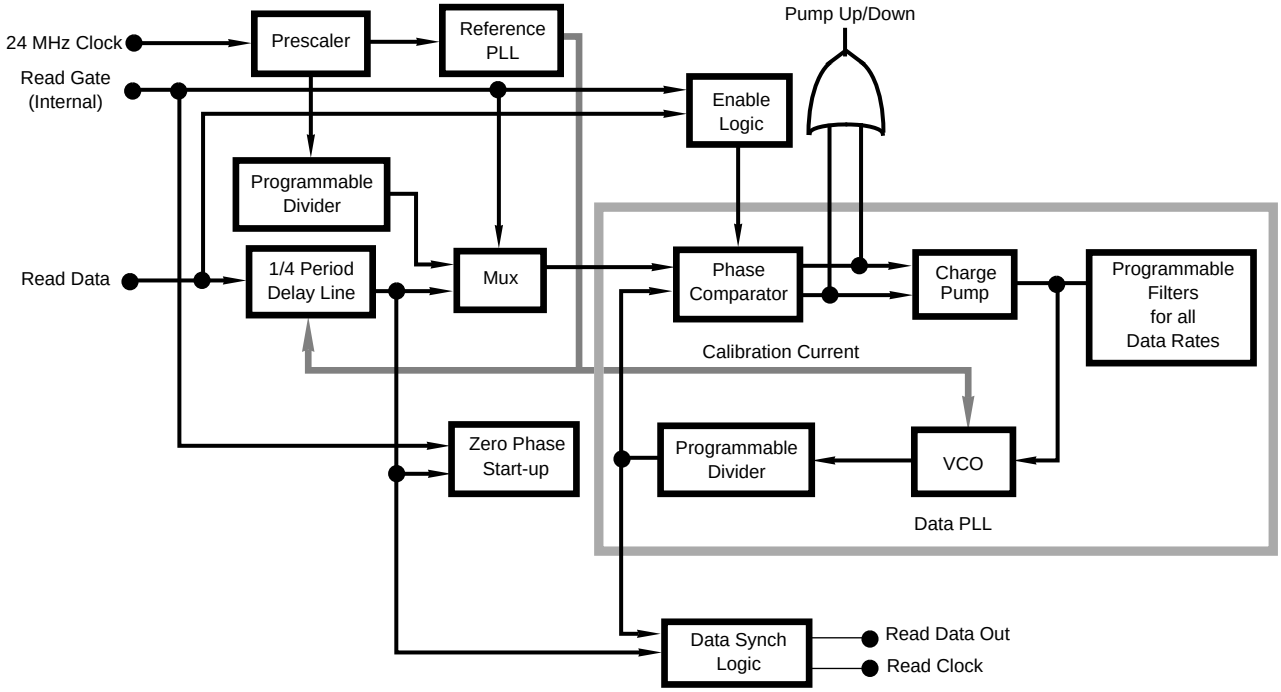


FIGURE 5-1. FDC Data Separator Block Diagram

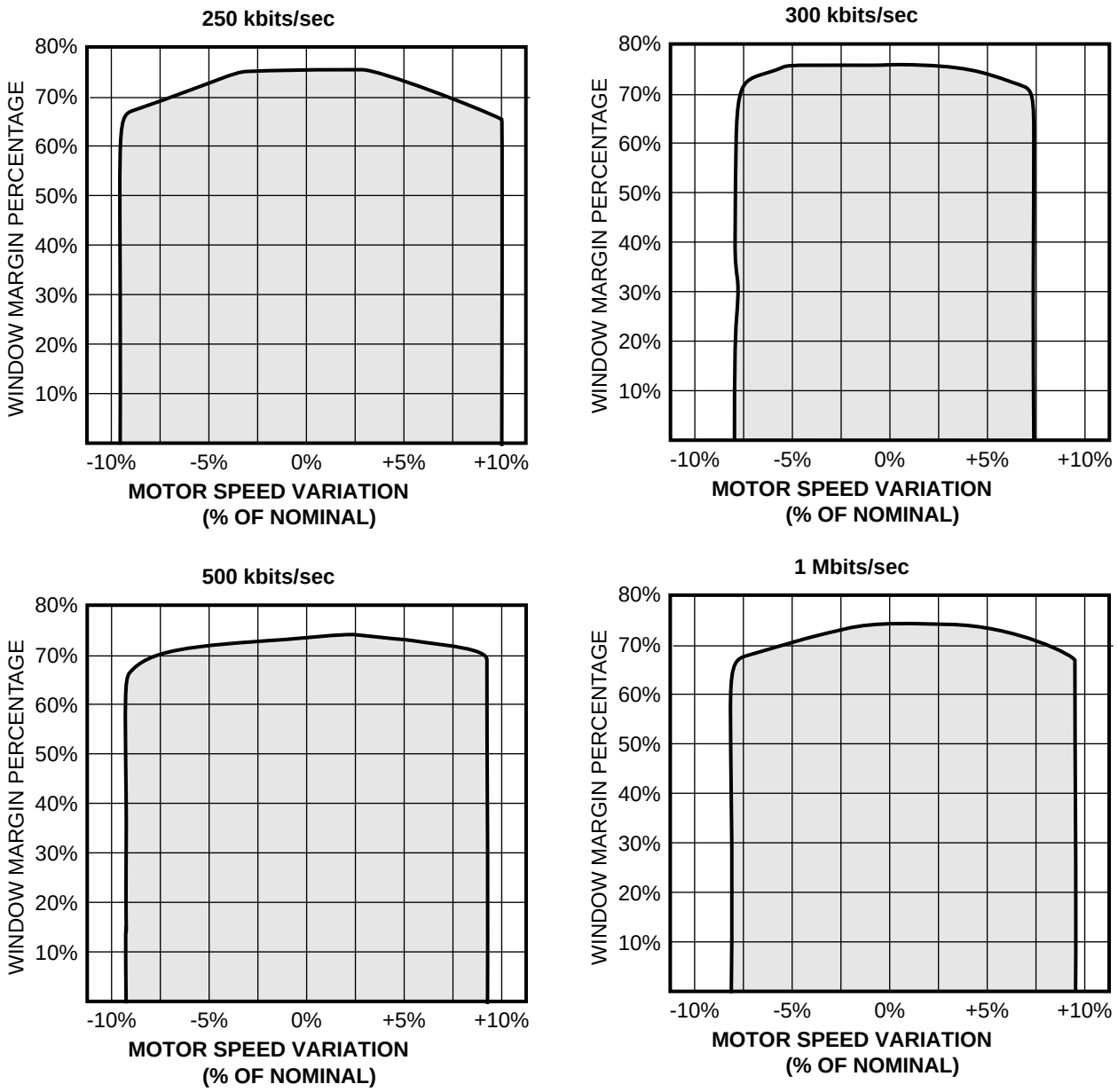


FIGURE 5-2. PC87308VUL Dynamic Window Margin Performance

(Typical performance at V_{DD} = 5.0V, 25 C)

5.1.5 Crystal Oscillator

When the clock of the FDC is an external 24 MHz source, the duty cycle of the external oscillator circuit must be between 40 to 60%, and must have minimum input voltages of 2.4 V for high level signals and 0.4 V for low level signals.

5.1.6 Perpendicular Recording Mode

The FDC is fully compatible with perpendicular recording mode disk drives at all data rates. These perpendicular mode drives are also called 4 Mbyte (unformatted) or 2.88 Mbyte (formatted) drives, which refers to their maximum storage capacity. Perpendicular recording will orient the magnetic flux changes (which represent bits) vertically on the disk surface, allowing for a higher recording density than the conventional longitudinal recording methods. With this increase in recording density comes an increase in the data rate of up to 1 Mbps, thus doubling the storage capacity. In addition, the perpendicular 2.88 M drive is read/write compatible with 1.44M and 720 K diskettes (500 Kbps and 250 Kbps respectively).

The 2.88 M drive has unique format and write data timing requirements due to its read/write head and pre-erase head design Figure 5-4. Unlike conventional disk drives which have only a read/write head, the 2.88 M drive has both a pre-erase head and read/write head. With conventional disk drives, the read/write head by itself is able to rewrite the disk without problems. For 2.88 M drives, a pre-erase head is needed to erase the magnetic flux on the disk surface before the read/write can write to the disk surface. The pre-erase head is activated during disk write operations only, i.e., Format and Write Data commands.

In 2.88 M drives, the pre-erase head leads the read/write head by 200 µm, which translates to 38 bytes at 1 Mb/s (19 bytes at 500 Kbps). For both conventional and perpendicular drives, WGATE is asserted with respect to the position of the read/write head. With conventional drives, this means that WGATE is asserted when the read/write head is located at the beginning of the Data Field preamble. With the 2.88 M drives, since the preamble must be pre-erased before it is rewritten, WGATE should be asserted when the pre-erase head is located at the beginning of the Data Field preamble. This means that WGATE should be asserted when the read/write head is at least 38 bytes (at 1 Mbps) before the preamble. See Table 5-14 on page 76 for a description of the WGATE timing for perpendicular drives at the various data rates.

Because of the 38 byte spacing between the read/write head and the pre-erase head at 1 Mbps, the GAP2 length of 22 bytes used in the standard IBM disk format is not long enough. There is a new format standard for 2.88M drives at 1 Mbps called the Perpendicular Format, which increases the GAP2 length to 41 bytes (see Figure 5-6 on page 72). The Perpendicular Mode command will put the floppy controller into perpendicular recording mode, which allows it to read and write perpendicular media. Once this command is invoked, the read, write and format commands can be executed in the normal manner. The perpendicular mode of the floppy controller will work at all data rates, adjusting the format and write data parameters accordingly. See “Perpendicular Mode Command” on page 75 for more details.

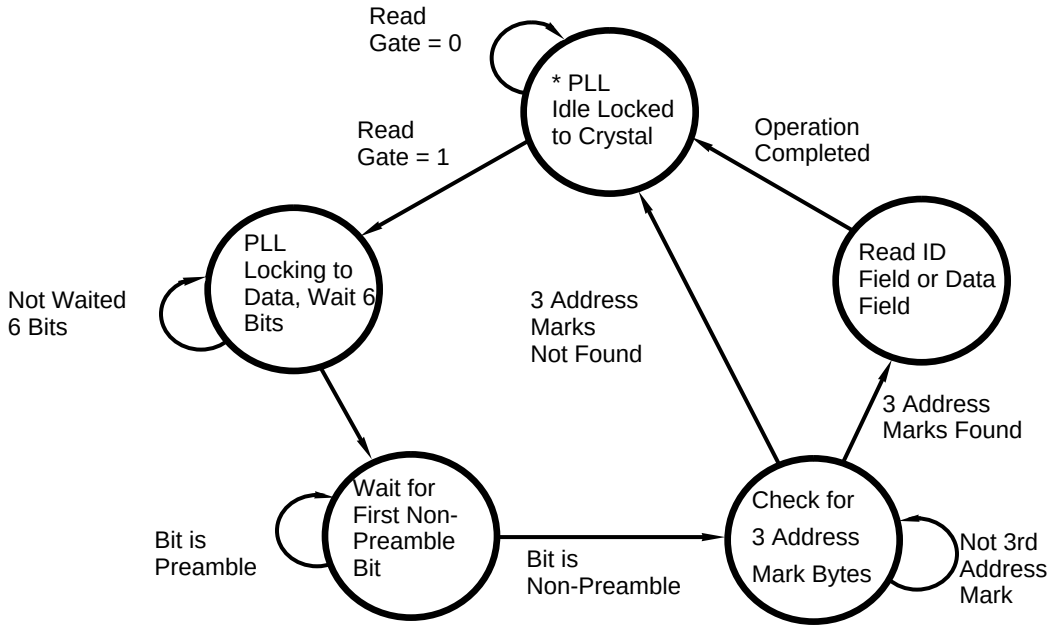


FIGURE 5-3. Read Data Algorithm - State Diagram

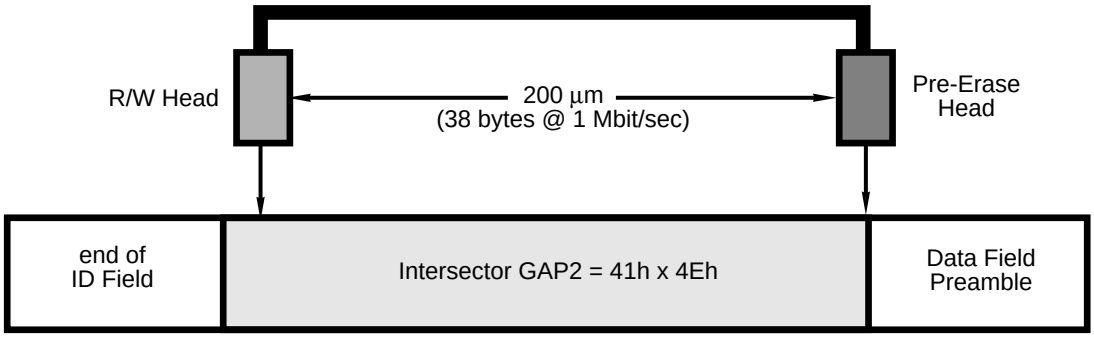


FIGURE 5-4. Perpendicular Recording Drive R/W Head and Pre-Erase Head

5.1.7 Data Rate Selection

The data rate can be chosen two different ways with the FDC. For PC compatible software, the Configuration Control Register at address 3F7h is used to program the data rate for the floppy controller. The lower bits D1 and D0 are used in the CCR to set the data rate. The other bits should be set to zero. See Table 5-6 on page 63 for the data rate select encoding.

The data rate can also be set using the Data Rate Select Register at address 4. Again, the lower two bits of the register are used to set the data rate. The encoding of these bits is exactly the same as those in the CCR. The remainder of the bits in the DSR are used for other functions. Consult the Register Description (Section 5.2.6 on page 63) for more details.

The data rate is determined by the last value that is written to either the CCR or the DSR. In other words, either the CCR or the DSR can override the data rate selection of the other register. When the data rate is selected, the micro-engine and data separator clocks are scaled appropriately. Also, the DRATE0 output pin will reflect the state of the data select bits that were last written to either the CCR or the DSR.

5.1.8 Write Precompensation

Write precompensation is a way of preconditioning the WDATA output signal to adjust for the effects of bit shift on the data as it is written to the disk surface. Bit shift is caused by the magnetic interaction of data bits as they are written to the disk surface, and has the effect of shifting these data bits away from their nominal position in the serial MFM or FM data pattern. Data that is subject to bit shift is much harder to read by a data separator, and can cause soft read errors. Write precompensation predicts where bit shift could occur within a data pattern. It then shifts the individual data bits early, late, or not at all such that when they are written to the disk, the resultant shifted data bits will be back in their nominal position.

The FDC supports software programmable write precompensation. Upon power up, the default write precompensation values are used (see Table 5-8 on page 64). The programmer can chose a different value of write precompensation with the DSR register if desired (see Table 5-7 on page 63). Also on power up, the default starting track number for write precompensation is track zero. This starting track number for write precompensation can be changed with the Configure command.

5.1.9 FDC Low Power Mode Logic

The FDC section of the PC87308VUL supports two low power modes described here in detail. Other low power modes of the PC87308VUL are described in Section 9.1 on page 158. Details concerning entering and exiting low power mode via setting Data Rate Select Register bit 6 or by executing the FDC Mode Command are covered below, in Section 5.2.6 on page 63 and “Mode Command” on page 74. The microcode is driven from the clock, so it will be disabled while the clock is off. The FDC clock is always disabled upon entering this mode. Upon entering the power down state, the RQM (Request For Master) bit in the MSR is cleared.

There are two modes of low power in the floppy controller: manual low power and automatic low power. Manual low power is enabled by writing a 1 to bit 6 of the DSR. The chip will go into low power immediately. This bit will be cleared to 0 after the chip is brought out of low power. Manual low power can also be accessed via the Mode command. The function of the manual low power mode is a logical OR function between the DSR low power bit and the Mode command manual low power bit setting.

Automatic low power mode will switch the controller into low power 500 ms (at the 500 Kbps MFM data rate) after it has entered the idle state. Once the auto low power mode is set, it does not have to be set again, and the controller will automatically go into low power mode after it has entered the idle state. Automatic low power mode can only be set with the Mode command.

There are two ways the FDC section can recover from the Power Down state. The part powers up after a software reset via the DOR or DSR. Since a software reset requires reinitialization of the controller, this method can be undesirable. The part also powers up after a read or write to either the Data Register or Main Status Register. This is the preferred method of power up since all internal register values are retained. It may take a few milliseconds for the oscillator to stabilize, and the µP will be prevented from issuing commands during this time through the normal Main Status Register protocol. That is, the RQM bit in the MSR will be a 0 until the oscillator has stabilized. When the controller has completely stabilized from power up, the RQM bit in the MSR is set to 1 and the controller can continue where it left off.

The Data Rate Select, Digital Output, and Configuration Control Registers are unaffected by the power down mode. They will remain active. It is up to the user to ensure that the Motor and Drive Select signals are turned off.

Note:

If the power to an external oscillator driving the PC87308VUL is to be independently removed during the FDC low power mode, it must not be done until 2 msec after the FDC low power command is issued.

5.1.10 Reset Operation

The floppy controller can be reset by hardware or software. Hardware reset is enacted by pulsing the Master Reset input pin. A hardware reset will set all of the user addressable registers and internal registers to their default values. The Specify command values will be don't cares, so they must be reinitialized. The major default conditions are: FIFO disabled, FIFO threshold = 0, Implied Seeks disabled, and Drive Polling enabled.

A software reset can be performed through the Digital Output Register or Data Rate Select Register. The DSR reset bit is self-clearing, while the DOR reset bit is not self-clearing. If the LOCK bit in the Lock command was set to a 1 previous to the software reset, the FIFO, THRESH, and PRETRK parameters in the Configure command will be retained. In addition, the FWR, FRD, and BST parameters in the Mode command will be retained if LOCK is set to 1. This function eliminates the need for total reinitialization of the controller after a software reset.

After a hardware (assuming the FDC is enabled) or software reset, the Main Status Register is immediately available for read access by the µP. It returns a 00h value until all the internal registers have been updated and the data separator is stabilized. When the controller is ready to receive a command byte, the MSR returns a value of 80h (Request for Master bit is set). The MSR is guaranteed to return the 80h value within 2.5 µsec after a hardware or software reset. All other user addressable registers other than the Main Status Register and Data Register (FIFO) can be accessed at any time, even while the part is in reset.

5.2 FDC REGISTER DESCRIPTION

The floppy disk controller is suitable for all PC-AT, EISA, PS/2, and general purpose applications. The operational mode (PC-AT or PS/2) of the FDC is determined by bit 6 of the SuperI/O FDC Configuration register (at index 0xF0) as described in Section 2.6.1 on page 23. AT mode is the default. DP8473 and N82077 software compatibility is provided. Key features include a 16-byte FIFO, PS/2 diagnostic register support, perpendicular recording mode, CMOS disk interface, and a high performance analog data separator.

The FDC is enhanced with full PnP ISA support. The FDC is a boot device. If CFG0 strap pin is 1 during reset then the FDC wakes up active (enabled) and the $\overline{\text{IRQ}}$ and DMA of the FDC are routed to IRQ, DRQ2 and $\overline{\text{DACK2}}$ pins.

The FDC supports the standard PC data rates of 250, 300, 500 Kbps and 1 Mbps in MFM-encoded data mode, but is no longer guaranteed through functional testing to support the older FM encoded data mode. References to the older FM mode remain in this document to clarify the true functional operation of the device.

The 1 Mbps data rate is used by the high performance tape and floppy drives emerging in the PC market today. The new floppy drives utilize high density media, which require the FDC-supported, perpendicular, recording mode format. When used with the 1 Mbps data rate, this new format allows the use of 4 MB floppy drives which format ED media to 2.88 MB capacity.

The high performance internal analog data separator needs no external components. It improves on the window margin performance standards of the DP8473, and is compatible with the strict data separator requirements of floppy and floppy-tape drives.

The FDC contains write precompensation circuitry that defaults to 125 nsec for 250, 300, and 500 Kbps (41.67 nsec at 1 Mbps). These values can be overridden in software to disable write precompensation or to provide levels of precompensation up to 250 nsec.

The FDC has internal 24 mA data bus buffers which allow direct connection to the system bus. The internal 40 mA totem-pole disk interface buffers are compatible with both CMOS drive input signals and 150Ω resistor terminated disk drive input signals.

The following FDC registers are mapped into the addresses shown in Table 5-1, with the base address range being provided by the on-chip address decoder pin. For PC-AT or PS/2 applications, the diskette controller primary address range is 3F0h to 3F7h, and the secondary address range is 370h to 377h.

The FDC supports two different register modes: the PC-AT mode and the PS/2 mode (MicroChannel systems). See Section 5.1.2 on page 52 for more details on how each register mode is enabled. When applicable, the register definition for each mode of operation is given. If no special notes are made, then the register is valid for both register modes.

TABLE 5-1. Register Descriptions and Addresses

A2	A1	A0	IDENT	R/W	Register	
0	0	0	0	R	Status Register A	SRA
0	0	1	0	R	Status Register B	SRB
0	1	0	x	R/W	Digital Output Register	DOR
0	1	1	x	R/W	Tape Drive Register	TDR
1	0	0	x	R	Main Status Register	MSR
1	0	0	x	W	Data Rate Select Register	DSR
1	0	1	x	R/W	Data Register (FIFO)	FIFO
1	1	0	x	X	None (Bus TRI-STATE)	
1	1	1	x	R	Digital Input Register	DIR
1	1	1	x	W	Configuration Control Register	CCR

Note: SRA and SRB are enabled in PS/2 mode only.

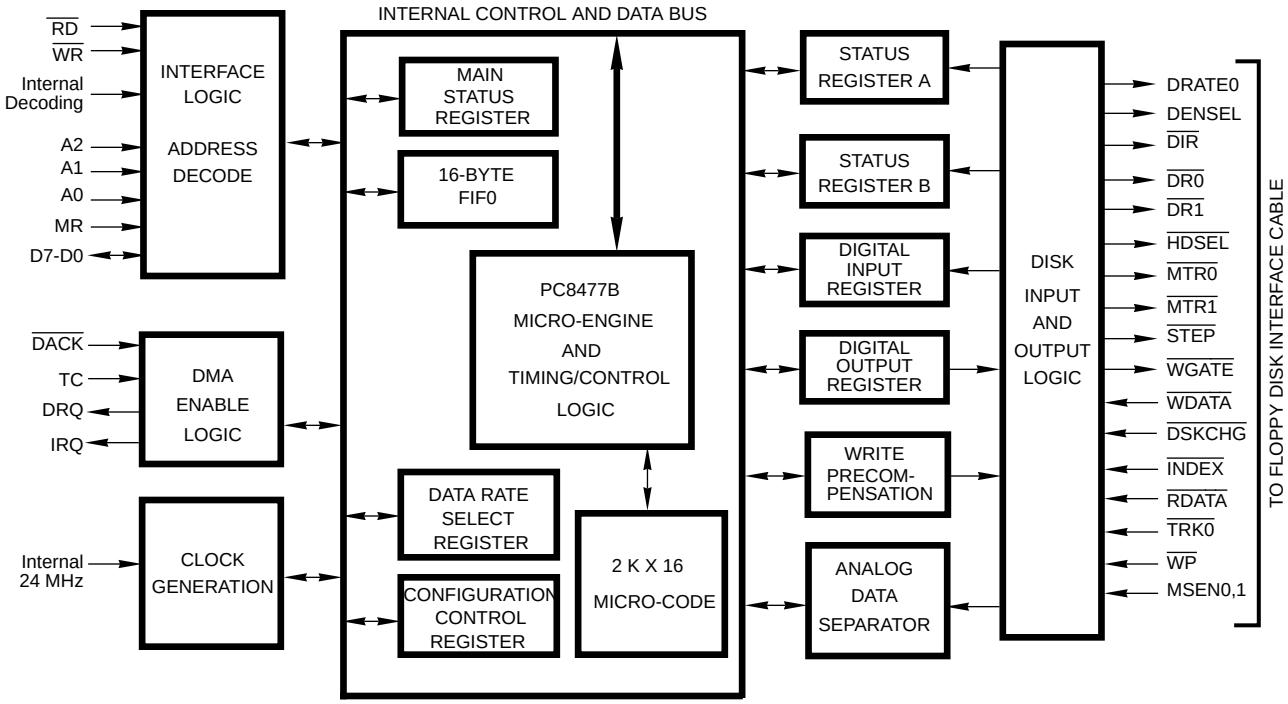


FIGURE 5-5. FDC Functional Block Diagram

5.2.1 Status Register A (SRA) Read Only

This read-only diagnostic register is part of the PS/2 floppy controller register set, and is enabled when in the PS/2 mode. This register monitors the state of the IRQ pin and some of the disk interface signals. The SRA can be read at any time when in PS/2 mode. In the PC-AT mode, D7-0 are TRI-STATE during a µP read.

SRA - PS/2 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	IRQ PEND	Res	STEP	$\overline{\text{TRK0}}$	HDSEL	$\overline{\text{INDX}}$	$\overline{\text{WP}}$	DIR
RESET COND	0	N/A	0	N/A	0	N/A	N/A	0

D0 **Direction:** Active high status of the DIR disk interface output.

D1 **$\overline{\text{Write Protect}}$:** Active low status of the WP disk interface input.

D2 **$\overline{\text{Index}}$:** Active low status of the INDEX disk interface input.

D3 **Head Select:** Active high status of the HDSEL disk interface output.

D4 **$\overline{\text{Track 0}}$:** Active low status of the TRK0 disk interface input.

D5 **Step:** Active high status of the STEP disk interface output.

D6 **Reserved**.

D7 **Interrupt Pending:** This active high bit reflects the state of the IRQ pin.

5.2.2 Status Register B (SRB) Read Only

This read-only diagnostic register is part of the PS/2 floppy controller register set, and is enabled when in the PS/2 mode. The SRB can be read at any time when in PS/2 mode. In the PC-AT mode, D7-D0 are TRI-STATE during a µP read.

SRB - PS/2 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	1	1	DR0	WDATA	RDATA	WGATE	MTR1	MTR**0**
RESET COND	N/A	N/A	0	0	0	0	0	0

D0 **Motor Enable 0:** Active high status of the MTR0 disk interface output. Low after a hardware reset, unaffected by a software reset.

D1 **Motor Enable 1:** Active high status of the MTR1 disk interface output. Low after a hardware reset, unaffected by a software reset.

D2 **Write Gate:** Active high status of the WGATE disk interface output.

D3 **Read Data:** Every inactive edge transition of the RDATA disk interface output causes this bit to change states.

D4 **Write Data:** Every inactive edge transition of the WDATA disk interface output causes this bit to change states.

D5 **Drive Select 0:** Reflects the status of the Drive Select 0 bit in the DOR (address 2, bit 0). It is cleared after a hardware reset, not a software reset.

D6 **Reserved:** Always 1.

D7 **Reserved:** Always 1.

5.2.3 Digital Output Register (DOR) Read/Write

The DOR controls the drive select and motor enable disk interface outputs, enables the DMA logic, and contains a software reset bit. The contents of the DOR is set to 00h after a hardware reset, and is unaffected by a software reset. The DOR can be written to at any time.

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	MTR3	MTR2	MTR1	MTR0	DMAEN	RESET	DRIVE SEL 1	DRIVE SEL 0
RESET COND	0	0	0	0	0	0	0	0

D1, 0 **Drive Select:** These two bits are binary encoded for the four drive selects DR3-0, so that only one drive select output is active at a time. See also logical drive exchange and four drive mode. DR3,2 are not connected to pins. They can be reproduced by external logic in four drive mode.

D2 **Reset Controller:** Writing a 0 to this bit resets the controller. It remains in the reset condition until a 1 is written to this bit. A software reset does not affect the DSR, CCR, and other bits of the DOR. A software reset affects the Configure and Mode command bits. See Section 5.3 on page 66. The minimum time that this bit must be low is 100 nsec. Thus, toggling the Reset Controller bit during consecutive writes to the DOR is an acceptable method of issuing a software reset.

D3 **DMA Enable:** This bit has two modes of operation:

PC-AT mode: Writing a 1 to this bit enables the DRQ, $\overline{\text{DACK}}$, TC, and IRQ pins. Writing a 0 to this bit disables the $\overline{\text{DACK}}$ and TC pins and TRI-STATE the DRQ and the IRQ pins. This bit is a 0 after a reset when in these modes.

PS/2 mode: This bit is reserved, and the DRQ, $\overline{\text{DACK}}$, TC, and IRQ pins are always enabled. During a reset, the DRQ, $\overline{\text{DACK}}$, TC, and IRQ lines remain enabled, and D3 is 0.

D4 **Motor Enable 0:** This bit controls the MTR0 disk interface output. A 1 in this bit causes the MTR0 pin to go active. See also logical drive exchange and four drive mode.

D5 **Motor Enable 1:** Same function as D7 except for MTR1. This bit controls the MTR1 disk interface output. A 1 in this bit causes the MTR1 pin to go active. See also logical drive exchange and four drive mode.

D6 **Motor Enable 2:** Same function as D7 except for MTR2. MTR2 is not connected to a SuperI/O pin; it can be reproduced by external logic in four drive mode.

D7 **Motor Enable 3:** This bit controls the MTR3 disk interface output. A 1 in this bit causes the MTR3 pin to go active. MTR3 is not connected to a SuperI/O pin; it can be reproduced by external logic in four drive mode.

It is common programming practice to enable both the motor enable and drive select output signals for a particular drive. Table 5-2 shows the DOR values to enable each of the four drives.

TABLE 5-2. Drive Enable Values

DRIVE	DOR VALUE
0	1Ch
1	2D
2	4E
3	8F

Note:

The MTR3, MTR2, DRV3, DRV2 are not connected to the PC87308VUL pins. They can be reproduced by external logic in four drive mode.

5.2.4 Tape Drive Register (TDR) Read/Write

The TDR register is the Tape Drive Register and the floppy disk controller media and drive type register. The register has two modes of operation (see Table 5-3).

Compatible AT TDR mode. The register is used to assign a particular drive number to the tape drive support mode of the data separator. All other logical drives can be assigned as floppy drive support. Bits 7-2 are in TRI-STATE during read operations.

Enhanced mode. This is the PS/2 TDR mode. It uses all the register's bits for operation with PS/2 floppy drives.

The use of the TDR bits, for each of these modes, is shown in Table 5-3.

D1, 0 **Tape Select 1,0:** These bits assign a logical drive number to a tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive. See Table 5-4 for the tape drive assignment values.

TABLE 5-3. TDR Operation Modes

Mode	SuperI/O FDC Configuration Register Bit 6	Bit	D7	D6	D5	D4	D3	D2	D1	D0
Compatible AT TDR	0	DESC	Float	Float	Float	Float	Float	Float	TAPE SEL 1	TAPE SEL 0
		RESET COND	N/A	N/A	N/A	N/A	N/A	N/A	0	0
Enhanced	1	DESC	ED	HD	Drive ID 1	Drive ID 0	SWP1	SWP0	TAPE SEL 1	TAPE SEL 0
		RESET COND	N/A	N/A	1	1	0	0	0	0

TABLE 5-4. Tape Drive Assignment Values

TAPESEL1	TAPESEL0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

D3,2 Bits 3 and 2 are read/write bits that control logical drive exchange. These bits allows software to exchange the physical floppy-disk control signals, assigned to pins.

When working with four drives, logical bit exchange is not encoded, i.e., bit 7 of the SuperI/O FDC Configuration register (at offset F0h) is not affected. (See Section 2.6.1 on page 23.)

00 : No logical drive exchange.

01 : Logical drive exchange between drives 0 and 1

$\overline{DR1}$ internal signal to $\overline{DR0}$ pin
$\overline{MTR1}$ internal signal to $\overline{MTR0}$ pin
$\overline{DR0}$ internal signal to $\overline{DR1}$ pin
$\overline{MTR0}$ internal signal to $\overline{MTR1}$ pin.

10 : Logical drive exchange between drives 0 and 2. The $\overline{DR0}$ and $\overline{MTR0}$ pins function is exchanged as follows:
$\overline{DR2}$ internal signal to $\overline{DR0}$ pin.
$\overline{MTR2}$ internal signal to $\overline{MTR0}$ pin.

11 : Reserved. Unpredictable results when 11 is configured.

D4 **Drive ID 0 Information:** Holds the information that is stored in the Drive ID register (Index F1h from Logical Device 3) as described in Section 2.6.2 on page 23.

D5 **Drive ID 1 Information:** Holds the information that is stored in the Drive ID register (Index F1h from Logical Device 3) as described in Section 2.6.2 on page 23.

D6 **High Density:** This media ID bit is used with bit 7 to indicate the type of media currently in the active floppy drive. This bit holds MSEN0 pin value. See Table 5-5 for details regarding bits 7,6.

TABLE 5-5. Media ID Bit Functions

Bit 7	Bit 6	Media Type
0	0	5.25 “
0	1	2.88 M
1	0	1.44 M
1	1	720 K

D7 **Extra Density:** This media ID bit is used with bit 6 to indicate the type of media currently in the active floppy drive. This bit holds MSEN1 pin value. See Table 5-5 for details regarding bits 7,6.

5.2.5 Main Status Register (MSR) Read Only

The read-only Main Status Register indicates the current status of the disk controller. The Main Status Register is always available to be read. One of its functions is to control the flow of data to and from the Data Register (FIFO). The Main Status Register indicates when the disk controller is ready to send or receive data through the Data Register. It should be read before each byte is transferred to or from the Data Register except during a DMA transfer. No delay is required when reading this register after a data transfer.

After a hardware or software reset, or recovery from a power down state, the Main Status Register is immediately available to be read by the µP. It contains a value of 00h until the oscillator circuit has stabilized, and the internal registers have been initialized. When the FDC is ready to receive a new command, it reports an 80h to the µP. The system software can poll the MSR until it is ready. The worst case time allowed for the MSR to report an 80h value (RQM set) is 2.5 µsec after reset or power up.

MSR

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	RQM	DIO	NON DMA	CMD PROG	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY
RESET COND	0	0	0	0	0	0	0	0

D0 **Drive 0 Busy:** Set after the last byte of the Command Phase of a Seek or Recalibrate command is issued for drive 0. Cleared after reading the first byte in the Result Phase of the Sense Interrupt Command for this drive.

D1 **Drive 1 Busy:** Same as above for drive 1.

D2 **Drive 2 Busy:** Same as above for drive 2.

D3 Drive 3 Busy: Same as above for drive 3.

D4 **Command in Progress:** This bit is set after the first byte of the Command Phase is written. This bit is cleared after the last byte of the Result Phase is read. If there is no Result Phase in a command, the bit is cleared after the last byte of the Command Phase is written.

D5 **Non-DMA Execution:** Indicates that the controller is in the Execution Phase of a byte transfer operation in the Non-DMA mode. Used for multiple byte transfers by the µP in the Execution Phase through interrupts or software polling.

D6 **Data I/O (Direction):** Indicates whether the controller is expecting a byte to be written to (0) or read from (1) the Data Register.

D7 **Request for Master:** Indicates that the controller is ready to send or receive data from the µP through the FIFO. This bit is cleared immediately after a byte transfer and is set again as soon as the disk controller is ready for the next byte. During a Non-DMA Execution phase, the RQM indicates the status of the interrupt pin.

5.2.6 Data Rate Select Register (DSR) Write Only

This write-only register is used to program the data rate, amount of write precompensation, power down mode, and software reset. The data rate is programmed via the CCR, not the DSR, for PC-AT and PS/2 applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is determined by the most recent write to either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset sets the DSR to 02h, which corresponds to the default precompensation setting and 250 Kbps.

DSR

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	S/W RESET	LOW POWER	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE1	DRATE0
RESET COND	0	0	0	0	0	0	1	0

D1,0 **Data Rate Select 1,0:** These bits determine the data rate for the floppy controller. See Table 5-6 for the corresponding data rate for each value of D1, D0. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

TABLE 5-6. Data Rate Select Encoding

DATA RATE SELECT		DATA RATE	
1	**0**	**MFM**	**FM**
1	1	1 Mbps	Illegal
0	0	500 Kbps	250 Kbps
0	1	300 Kbps	150 Kbps
1	0	250 Kbps	125 Kbps

Note:

FM mode is not guaranteed through functional testing.

D4-2 **Precompensation Select:** These three bits select the amount of write precompensation the floppy controller uses on the WDATA disk interface output. Table 5-7 shows the amount of precompensation used for each bit pattern. In most cases, the default values (Table 5-8) can be used; however, alternate values can be chosen for specific types of drives and media. Track 0 is the default starting track number for precompensation. The starting track number can be changed in the Configure command.

TABLE 5-7. Write Precompensation Delays

PRECOMP 432	PRECOMPENSATION DELAY
111	0.0 ns
001	41.7 ns
010	83.3 ns
011	125.0 ns
100	166.7 ns
101	208.3 ns
110	250.0 ns
000	DEFAULT

TABLE 5-8. Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAY
1 Mbps	41.7 ns
500 Kbps	125.0 ns
300 Kbps	125.0 ns
250 Kbps	125.0 ns

D5 Undefined. Should be set to 0.

D6 **Low Power:** A 1 to this bit puts the controller into the Manual Low Power mode. The oscillator and data separator circuits are turned off. Manual Low Power can also be accessed via the Mode command. The chip comes out of low power after a software reset, or access to the Data Register or Main Status Register.

D7 **Software Reset:** This bit has the same function as the DOR RESET (D2) except that this software reset is self-clearing.

5.2.7 Data Register (FIFO) Read/Write

The FIFO (read/write) is used to transfer all commands, data, and status between the µP and the FDC. During the Command Phase, the µP writes the command bytes into the FIFO after polling the RQM and DIO bits in the MSR. During the Result Phase, the µP reads the result bytes from the FIFO after polling the RQM and DIO bits in the MSR.

Enabling the FIFO, and setting the FIFO threshold, is done via the Configure command. If the FIFO is enabled, only the Execution Phase byte transfers use the 16-byte FIFO. The FIFO is always disabled during the Command and Result Phases of a controller operation. If the FIFO is enabled, it is not disabled after a software reset if the LOCK bit is set in the Lock Command. After a hardware reset, the FIFO is disabled to maintain compatibility with PC-AT systems.

The 16-byte FIFO can be used for DMA, Interrupt, or software polling type transfers during the execution of a read, write, format, or scan command. In addition, the FIFO can be put into a Burst or Non-Burst mode with the Mode command.

In the Burst mode, DRQ or IRQ remains active until all of the bytes have been transferred to or from the FIFO. In the Non-Burst mode, DRQ or IRQ is deasserted for 350 ns to allow higher priority transfer requests to be serviced.

The Mode command can also disable the FIFO for either reads or writes separately. The FIFO allows the system a larger latency without causing a disk overrun/underrun error. Typical uses of the FIFO are at the 1 Mbps data rate, or with multi-tasking operating systems. The default state of the FIFO is disabled, with a threshold of zero. The default state is entered after a hardware reset.

Data Register (FIFO)

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	Data [7:0]							
RESET COND	Byte Mode							

During the Execution Phase of a command involving data transfer to/from the FIFO, the system must respond to a data transfer service request based on the following formula:

Maximum Allowable Data Transfer Service Time

(THRESH + 1) x 8 x t_{DRP} – (16 x t_{ICP})

This formula is good for all data rates with the FIFO enabled or disabled. THRESH is a four bit value programmed in the Configure command, which sets the FIFO threshold. If the FIFO is disabled, THRESH is zero in the above formula. The last term of the formula, (16 x t_{ICP}) is an inherent delay due to the microcode overhead required by the FDC. This delay is also data rate dependent. See Table 9-1 for the t_{DRP} and t_{ICP} times.

The programmable FIFO threshold (THRESH) is useful in adjusting the floppy controller to the speed of the system. In other words, a slow system with a sluggish DMA transfer capability uses a high value of THRESH, giving the system more time to respond to a data transfer service request (DRQ for DMA mode or IRQ for Interrupt mode). Conversely, a fast system with quick response to a data transfer service request uses a low value of THRESH.

5.2.8 Digital Input Register (DIR) Read Only

This diagnostic register is used to detect the state of the DSKCHG disk interface input and some diagnostic signals. The function of this register depends on the register mode of operation. When in the PC-AT mode, D6-D0 are TRI-STATE to avoid conflict with the fixed disk status register at the same address. DIR is unaffected by a software reset.

DIR - PC-AT Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	DSKCHG	X	X	X	X	X	X	X
RESET COND	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

D6-0 **Undefined:** TRI-STATE. Used by Hard Disk Controller Status Register.

D7 **Disk Changed:** Active high status of DSKCHG disk interface input. During power down this bit is invalid, if it is read by the software.

DIR - PS/2 Mode

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	DSKCHG	1	1	1	1	DRATE1	DRATE0	$\overline{\text{HIGH}}$ $\overline{\text{DEN}}$
RESET COND	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

D0 **$\overline{\text{High Density}}$:** This bit is low when the 1 Mb/s or 500 Kbps data rate is chosen, and high when the 300 Kbps or 250 Kbps data rate is chosen.This bit is independent of the IDENT value.

D2,1 **Data Rata Select 1,0:** These bits indicate the status of the DRATE1-0 bits programmed through the DSR or CCR.

D6-3 **Reserved:** Always 1.

D7 **Disk Changed:** Active high status of DSKCHG disk interface input. During power down this bit is invalid, if it is read by the software.

5.2.9 Configuration Control Register (CCR) Write Only

This is the write-only data rate register commonly used in PC-AT applications. This register is not affected by a software reset, and is set to 250 Kbps after a hardware reset. The data rate of the floppy controller is determined by the last write to either the CCR or DSR.

CCR

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	0	0	0	0	0	0	DRATE1	DRATE0
RESET COND	N/A	N/A	N/A	N/A	N/A	N/A	1	0

D1,0 **Data Rate Select 1,0:** These bits determine the data rate of the floppy controller. See Table 5-6 for the appropriate values.

D7-2 **Reserved:** Should be set to 0.

5.2.10 Result Phase Status Registers

The Result Phase of a command contains bytes that hold status information. The format of these bytes are described below. Do not confuse these status bytes with the Main Status Register, which is a read only register that is always valid. The Result Phase status registers are read from the Data Register (FIFO) only during the Result Phase of certain commands. See Section 5.3.1 on page 66. The status of each register bit is indicated when the bit is 1.

Status Register 0 (ST0)

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	IC	IC	SE	EC	0	HDS	DS1	DS0
RESET COND	0	0	0	0	0	0	0	0

D1,0 **Drive Select 1,0:** These two binary encoded bits indicate the logical drive selected at the end of the Execution Phase.

00 = Drive 0 selected.

01 = Drive 1 selected.

10 = Drive 2 selected.

11 = Drive 3 selected.

MTR3,2 and DR3,2 are not connected to pins. They can be reproduced by external logic in four drive mode.

D2 **Head Select:** Indicates the active high status of the HDSEL pin at the end of the Execution Phase.

D3 Not used. Always 0.

D4 **Equipment Check:** After a Recalibrate command, Track 0 signal failed to occur. (Used during Sense Interrupt command).

D5 **Seek End:** Seek, Relative Seek, or Recalibrate command completed by the controller. (Used during a Sense Interrupt command).

D7,6 Interrupt Code:

00 = Normal Termination of Command.

01 = Abnormal Termination of Command: Execution of command was started, but was not successfully completed.

10 = Invalid Command issued: Command issued was not recognized as a valid command.

11 = Internal drive ready status changed state during the drive polling mode: Only occurs after a hardware or software reset.

Status Register 1 (ST1)

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	ET	0	CE	OR	0	ND	NW	MA
RESET COND	0	0	0	0	0	0	0	0

D0 **Missing Address Mark:** If bit 0 of ST2 is clear then the controller cannot detect any Address Field Address Mark after two disk revolutions. If bit 0 of ST2 is set then the controller cannot detect the Data Field Address Mark after finding the correct Address Field.

D1 **Not Writable:** Write Protect pin is active when a Write or Format command is issued.

D2 **No Data:** Three possible problems:

1) Controller cannot find the sector specified in the Command Phase during the execution of a Read, Write, Scan, or Verify command. An address mark was found however, so it is not a blank disk.

2) Controller cannot read any Address Fields without a CRC error during a Read ID command.

3) Controller cannot find starting sector during execution of Read A Track command.

D3 Not used. Always 0.

D4 **Overrun:** Controller was not serviced by the µP soon enough during a data transfer in the Execution Phase. For read operations, indicates a data overrun. For write operations, indicates a data underrun.

D5 **CRC Error:** If this bit is set and bit 5 of ST2 is clear, then there was a CRC error in the Address Field of the correct sector. If bit 5 of ST2 is also set, then there was a CRC error in the Data Field.

D6 Not used. Always 0.

D7 **End of Track:** Controller transferred the last byte of the last sector without the TC pin becoming active. The last sector is the End of Track sector number programmed in the Command Phase.

Status Register 2 (ST2)

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	0	CM	CD	WT	SEH	SNS	BT	MD
RESET COND	0	0	0	0	0	0	0	0

D0 **Missing Address Mark in Data Field:** Controller cannot find the Data Field AM during a Read, Scan, or Verify command. Bit 0 of ST1 is also set.

D1 **Bad Track:** Only set if the desired sector is not found, the track number recorded on any sector on

the track is FFh indicating a hard error in IBM format, and is different from the track address specified in the Command Phase.

D2 **Scan Not Satisfied:** Controller cannot find a sector on the track which meets the desired condition during any Scan command.

D3 **Scan Equal Hit:** "Equal" condition satisfied during any Scan command.

D4 **Wrong Track:** Only set if desired sector is not found, and the track number recorded on any sector of the current track is different from the track address specified in the Command Phase.

D5 **CRC Error in Data Field:** Controller detected a CRC error in the Data Field. Bit 5 of ST1 is also set.

D6 **Control Mark:** Controller tried to read a sector which contained a deleted data address mark during execution of Read Data or Scan commands. Or, if a Read Deleted Data command was executed, a regular address mark was detected.

D7 Not Used. Always 0.

Status Register 3 (ST3))

	D7	D6	D5	D4	D3	D2	D1	D0
DESC	0	WP	1	TK0	1	HDS	DS1	DS0
RESET COND	0	0	1	0	1	0	0	0

D1,0 Drive Select 1,0: These two binary encoded bits indicate the DS1-DS0 bits in the Command Phase.

D2 **Head Select:** Indicates the active high status of the HD bit in the Command Phase.

D3 Not used. Always 1.

D4 **Track 0:** Indicates active high status of the TRK0 pin.

D5 Not used. Always 1.

D6 **Write Protect:** Indicates active high status of the WP pin.

D7 Not used. Always 0.

5.3 DESCRIPTION OF THE FDC COMMAND SET

The following is a table of the FDC command set. Each command contains a unique first command byte, the opcode byte, which identifies to the controller how many command bytes to expect. If an invalid command byte is issued to the controller, it immediately enters the Result Phase and the status is 80h, signifying Invalid Command.

5.3.1 Command Set Summary

CONFIGURE

Command Phase

0	0	0	1	0	0	1	1
0	0	0	0	0	0	0	0
0	EIS	FIFO	POLL	THRESH			
PRETRK							

Execution Phase: Internal registers written.

No Result Phase

DUMPREG

Command Phase

0	0	0	0	1	1	1	0

Execution Phase: Internal registers read.

Result Phase

PTR Drive 0							
PTR Drive 1							
PTR Drive 2							
PTR Drive 3							
Step Rate Time				Motor Off Time			
Motor On Time							DMA
Sector per Track/End of Track							
LOCK	0	DC3	DC2	DC1	DC0	GAP	WG
0	EIS	FIFO	POLL	THRESH			
PRETRK							

Note: Sectors per Track parameter returned if last command issued was Format. End of Track parameter returned if last command issued was Read or Write.

FORMAT TRACK

Command Phase

0	MFM	0	0	1	1	0	1
X	X	X	X	X	HD	DR1	DR0
Bytes per Sector							
Sectors per Track							
Format Gap							
Data Pattern							

Execution Phase: System transfers four ID bytes (track, head, sector, bytes/sector) per sector to the floppy controller via DMA or Non-DMA modes. The entire track is formatted. The data block in the Data Field of each sector is filled with the data pattern byte.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Undefined
Undefined
Undefined
Undefined

INVALID

Command Phase

Invalid Op Codes

Result Phase

Status Register 0 (80 h)

LOCK

Command Phase

LOCK	0	0	1	0	1	0	0

Execution Phase: Internal register is written.

Result Phase

0	0	0	LOCK	0	0	0	0

MODE

Command Phase

0	0	0	0	0	0	0	1
TMR	IAF	IPS	0	LOW PWR		1	ETR
FWR	FRD	BST	R255	0	0	0	0
DENSEL		BFR	WLD	Head Settle			
0	0	0	0	0	RG	0	X

Execution Phase: Internal registers are written.

No Result Phase

NSC

Command Phase

0	0	0	1	1	0	0	0

Result Phase

0	1	1	1	0	0	1	1

PERPENDICULAR MODE

Command Phase

0	0	0	1	0	0	1	0
OW	0	DC3	DC2	DC1	DC0	GAP	WG

Execution Phase: Internal registers are written.

No Result Phase

READ DATA

Command Phase

MT	MFM	SK	0	0	1	1	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes Per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ DELETED DATA

Command Phase

MT	MFM	SK	0	1	1	0	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes Per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ ID

Command Phase

0	MFM	0	0	1	0	1	0
X	X	X	X	X	HD	DR1	DR0

Execution Phase: Controller reads first ID Field header bytes it can find and reports these bytes to the system in the result bytes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ A TRACK

Command Phase

0	MFM	0	0	0	0	1	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes Per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

RECALIBRATE

Command Phase

0	0	0	0	0	1	1	1
0	0	0	0	0	0	DR1	DR0

Execution Phase: Disk drive head is stepped out to Track 0.

No Result Phase

RELATIVE SEEK

Command Phase

1	DIR	0	0	1	1	1	1
X	X	X	X	X	HD	DR1	DR0
Relative Track Number							

Execution Phase: Disk drive head stepped in or out a programmable number of tracks.

No Result Phase

SCAN EQUAL

Command Phase

MT	MFM	SK	1	0	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes Per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Execution Phase: Data transferred from system to controller is compared to data read from disk.

Result Phase

MT	MFM	SK	1	1	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes Per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

SCAN HIGH OR EQUAL

Command Phase

MT	MFM	SK	1	1	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes Per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Execution Phase: Data transferred from system to controller is compared to data read from disk.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

SCAN LOW OR EQUAL

Command Phase

MT	MFM	SK	1	1	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes Per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Execution Phase: Data transferred from system to controller is compared to data read from disk.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

SEEK

Command Phase

0	0	0	0	1	1	1	1
X	X	X	X	X	HD	DR1	DR0
New Track Number							
MSN of Track Number				0	0	0	0

Note: Last Command Phase byte is required only if ETR is set in Mode Command.

Execution Phase: Disk drive head is stepped in or out to a programmable track.

No Result Phase

SENSE DRIVE STATUS

Command Phase

0	0	0	0	0	1	0	0
X	X	X	X	X	HD	DR1	DR0

Execution Phase: Disk drive status information is detected and reported.

Result Phase

Status Register 3

SENSE INTERRUPT

Command Phase

0	0	0	0	1	0	0	0

Execution Phase: Status of interrupt is reported.

Result Phase

Status Register 0				
Present Track Number (PTR)				
MSN of PTR	0	0	0	0

Note: Third Result Phase byte can only be read if ETR is set in the Mode Command.

SET TRACK

Command Phase

0	WNR	1	0	0	0	0	1
0	0	1	1	0	MSB	DR1	DR0
New Track Number (PTR)							

Execution Phase: Internal register is read or written.

Result Phase

Value

SPECIFY

Command Phase

0	0	0	0	0	0	1	1
Step Rate Time				Motor Off Time			
Motor On Time							DMA

Execution Phase: Internal registers are written.

No Result Phase

VERIFY

Command Phase

MT	MFM	SK	1	0	1	1	0
EC	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes Per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length/Sector Court							

Execution Phase: Data is read from disk but not transferred to the system.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

VERSION

Command Phase

0	0	0	1	0	0	0	0

Result Phase

1	0	0	1	0	0	0	0

WRITE DATA

Command Phase

MT	MFM	0	0	0	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes Per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data is transferred from the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

WRITE DELETED DATA

Command Phase

MT	MFM	0	0	1	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes Per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Execution Phase: Data is transferred from the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

5.3.2 Command Descriptions

Configure Command

The Configure Command controls some operation modes of the controller. It should be issued during the initialization of the FDC after power up. The function of the bits in the Configure registers are described below. These bits are set to their default values after a hardware reset. The value of each bit after a software reset is explained. The default value of each bit is denoted by a "bullet" to the left of the item.

EIS: Enable Implied Seeks. Default after a software reset.

- **0** = Implied seeks disabled through Configure command. Implied seeks can still be enabled through the Mode command when EIS = 0. (default)

  1 = Implied seeks enabled for a read, write, scan, or verify operation. A seek and sense interrupt operation is performed prior to the execution of the read, write, scan, or verify operation. The IPS bit does not need to be set.

FIFO: Enable FIFO for Execution Phase data transfers. Default after a software reset if the LOCK bit is 0. If the LOCK bit is 1, then the FIFO bit retains its previous value after a software reset.

  0 = FIFO enabled for both reads and writes.

- **1** = FIFO disabled. (default)

POLL: Disable for Drive Polling Mode. Default after a software reset.

- **0** = Enable polling mode. An interrupt is generated after a reset. (default)

  1 = Disable drive polling mode. If the Configure command is issued within 500 µs of a hardware or software reset, then an interrupt is not generated. In addition, the four Sense Interrupt commands to clear the “Ready Changed State” of the four logical drives is not required.

THRESH: The FIFO threshold in the Execution Phase of read and write data transfers. Programmable from 00h to 0Fh. Defaults to 00h after a software reset if the LOCK bit is 0. If the LOCK bit is 1, THRESH retains its value. A high value of THRESH is suited for slow response systems, and a low value of THRESH is better for fast response systems.

PRETRK: Starting track number for write precompensation. Programmable from track 0 (“00”) to track 255 (“FF”). Defaults to track 0 (“00”) after a software reset if the LOCK bit is 0. If the LOCK bit is 1, PRETRK retains its value.

Dumpreg Command

The Dumpreg command is designed to support system runtime diagnostics and application software development and debug. This command has a one-byte command phase and a 10-byte result phase, which return the values of parameters set in other commands. That is, the PTR (Present Track Register) contains the least significant byte of the track the microcode has stored for each drive. The Step Rate Time, Motor Off and Motor On Times, and the DMA bit are all set in the Specify command.

The sixth byte of the result phase varies depending on what commands have been previously executed. If a format command has previously been issued, and no reads or writes have been issued since then, this byte contains the Sectors per track value. If a read or a write command has been executed more recently than a format command, this byte contains the End of Track value. The LOCK bit is set in the Lock command. The eighth result byte also contains the bits programmed in the Perpendicular Mode command. The last two bytes of the Dumpreg Result Phase are set in the Configure command. After a hardware or software reset, the parameters in the result bytes are set to their appropriate default values.

Note: Some of these parameters are unaffected by a software reset, depending on the state of the LOCK bit.

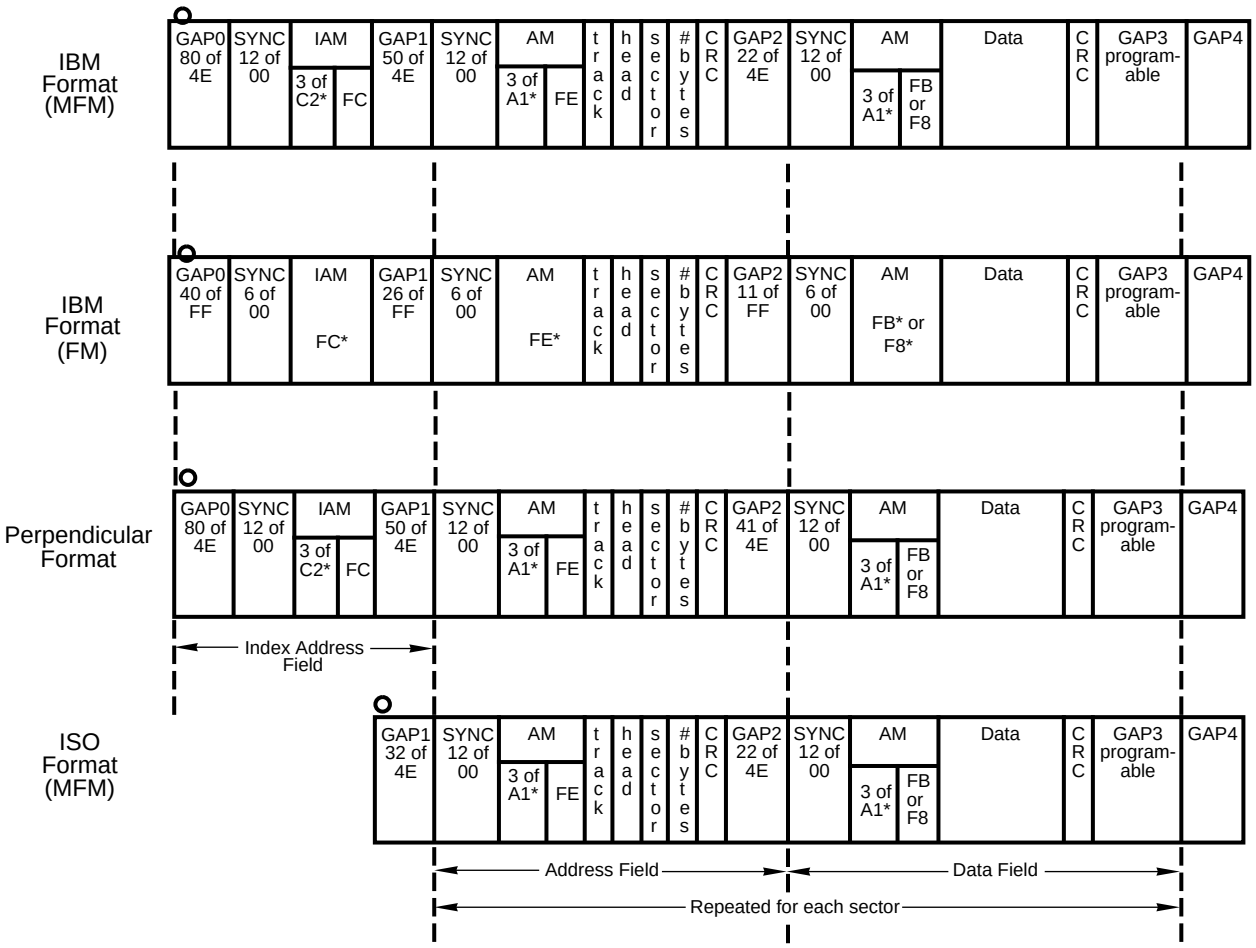
Format Track Command

This command formats one track on the disk in IBM, ISO, or Perpendicular Format. After the index hole is detected, data patterns are written on the disk including all gaps, address marks, Address Fields, and Data Fields. The exact format is determined by the following parameters:

1. The MFM bit in the Opcode (first command) byte, which determines the format of the Address Marks and the encoding scheme.
2. The IAF bit in the Mode command, which selects between IBM and ISO format.
3. The WGATE and GAP bits in the Perpendicular Mode command, which select between the conventional and Toshiba Perpendicular format.
4. The Bytes per Sector code, which determines the sector size.
5. The Sector per Track parameter, which determines how many sectors are formatted on the track.
6. The Data Pattern byte, which is used as the filler byte in the Data Field of each sector.

To allow for flexible formatting, the µP must supply the four Address Field bytes (track, head, sector, bytes per sector code) for each sector formatted during the Execution Phase. This allows for non-sequential sector interleaving. This transfer of bytes from the µP to the controller can be done in the DMA or Non-DMA mode, with the FIFO enabled or disabled.

The Format command terminates when the index hole is detected a second time, at which point an interrupt is generated. Only the first three status bytes in the Result Phase are significant. The Format Gap byte in the Command Phase is dependent on the data rate and type of disk drive, and controls the length of GAP3. Some typical values for the programmable GAP3 are given in 5-9 on page 73. Figure 5-6 shows the track format for each of the formats recognized by the format command.



Notes:

FE* = Data Pattern of FE, Clock Pattern of C7

FC* = Data Pattern of FC, Clock Pattern of D7

FB* = Data Pattern of FB, Clock Pattern of C7

F8* = Data Pattern of F8, Clock Pattern of C7

A1* = Data Pattern of A1, Clock Pattern of 0A

C2* = Data Pattern of C2, Clock Pattern of 14

All byte counts in decimal notation

All byte values in are in hexadecimal notation

CRC uses standard polynomial $x^{16} + x^{12} + x^{5} + 1$

FM mode is not guaranteed through functional testing

Perpendicular Format GAP2 = 41 bytes for 1 Mb/s.

All other data rates use GAP2 = 22 bytes

FIGURE 5-6. IBM, Perpendicular, and ISO Formats Supported by Format Command

TABLE 5-9. Typical Format Gap Length Values

MODE	SECTOR SIZE decimal	SECTOR CODE hex	EOT hex	SECTOR GAP hex	FORMAT GAP3 hex
	128	00	12	07	09
	128	00	10	10	19
125 Kbps	256	01	08	18	30
FM	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
	256	01	12	0A	0C
	256	01	10	20	32
250 Kbps	512	02	08	2A	50
MFM	512	02	09	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
	128	00	1A	07	1B
	256	01	0F	0E	2A
250 Kbps	512	02	08	1B	3A
FM	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
500 Kbps	256	01	1A	0E	36
MFM	512	02	0F	1B	54
	512	02	12	1B	6C
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF

TABLE 5-10. Typical Values for PC Compatible Diskette Media

MEDIA TYPE	SECTOR SIZE decimal	SECTOR CODE hex	EOT hex	SECTOR GAP hex	FORMAT GAP3 hex
360K	512	02	09	2A	50
1.2M	512	02	0F	1B	54
720K	512	02	09	1B	50
1.44M	512	02	12	1B	6C
2.88M	512	02	24	1B	53

Notes:

1. Sector Gap refers to the Intersector Gap Length parameter specified in the Command Phase of the Read, Write, Scan, and Verify commands. Although this is the recommended value, the FDC treats this byte as a don't care in the Read, Write, Scan, and Verify commands.
2. Format Gap is the suggested value to use in the Format Gap parameter of the Format command. This is the programmable GAP3 as shown in Figure 5-6.
3. The 2.88M diskette media is a Barium Ferrite media intended for use in Perpendicular Recording drives at the data rate of up to 1 Mb/s.

Invalid Command

If an invalid command (illegal Opcode byte in the Command Phase) is received by the controller, the controller responds with ST0 in the Result Phase. The controller does not generate an interrupt during this condition. Bits 6 and 7 in the MSR are both set to a 1, indicating to the µP that the controller is in the Result Phase and the contents of ST0 must be read. The system reads an 80h value from ST0 indicating an invalid command was received.

Lock Command

The Lock command allows the user full control of the FIFO parameters after a software reset. If the LOCK bit is set to 1, then the FIFO, THRESH, and PRETRK bits in the Configure command are not affected by a software reset. In addition, the FWR, FRD, and BST bits in the Mode command is unaffected by a software reset. If the LOCK is 0 (default after a hardware reset), then the above bits are set to their default values after a software reset. This command is useful if the system designer wishes to keep the FIFO enabled and retain the other FIFO parameter values (such as THRESH) after a software reset.

After the command byte is written, the result byte must be read before continuing to the next command. The execution of the Lock command is not performed until the result byte is read by the µP. If the part is reset after the command byte is written but before the result byte is read, then the Lock command execution is not performed. This is done to prevent accidental execution of the Lock command.

Mode Command

This command is used to select the special features of the controller. The bits for the Command Phase bytes are shown in Section 5.3.1 on page 66, Command Set Summary, and their function is described below. These bits are set to their default values after a hardware reset. The default value of each bit is denoted by a "bullet" to the left of the item. The value of each parameter after a software reset is explained.

TMR: Motor Timer mode. Default after a software reset.

- **0** = Timers for motor on and motor off are defined for Mode 1. (See Specify command). (default)

  1 = Timers for motor on and motor off are defined for Mode 2. (See Specify command).

IAF: Index Address Format. Default after a software reset.

- **0** = The controller formats tracks with the Index Address Field included. (IBM and Perpendicular format).

  1 = The controller formats tracks without including the Index Address Field. (ISO format).

IPS: Implied Seek. Default after a software reset.

- **0** = The implied seek bit in the command byte of a read, write, scan, or verify is ignored. Implied seeks could still be enabled by the EIS bit in the Configure command.

  1 = The IPS bit in the command byte of a read, write, scan, or verify is enabled so that if it is set, the controller performs seek and sense interrupt operations before the executing the command.

LOW PWR: Low Power mode. Default after a software reset.

- **00** = Completely disable the low power mode. (default)

  01 = Automatic low power. Go into low power mode 512 ms after the head unload timer times out. (This assumes a 500 Kbps data rate) For 250 Kbps the time-out period is double to 1 s.

  10 = Manual low power. Go into low power mode now.

  11 = Not used.

ETR: Extended Track Range. Default after a software reset.

- **0** = Track number is stored as a standard 8-bit value compatible with the IBM, ISO, and Perpendicular formats. This allows access of up to 256 tracks during a seek operation.

  1 = Track number is stored as a 12-bit value. The upper four bits of the track value are stored in the upper four bits of the head number in the sector Address Field. This allows access of up to 4096 tracks during a seek operation. With this bit set, an extra byte is required in the Seek Command Phase and Sense Interrupt Result Phase.

FWR: FIFO Write Disable for µP write transfers to controller. Default after a software reset if LOCK is 0. If LOCK is 1, FWR retains its value after a software reset.

Note: This bit is only valid if the FIFO is enabled in the Configure command. If the FIFO is not enabled in the Configure command, then this bit is a don't care.

- **0** = Enable FIFO. Execution Phase µP write transfers use the internal FIFO. (default)

  1 = Disable FIFO. All write data transfers take place without the FIFO.

FRD: FIFO Read Disable for µP read transfer from controller. Default after a software reset if LOCK is 0. If LOCK is 1, FRD retains its value after a software reset.

Note: This bit is only valid if the FIFO is enabled in the Configure command. If the FIFO is not enabled in the Configure command, then this bit is a don't care.

- **0** = Enable FIFO. Execution Phase µP read transfer use the internal FIFO. (default)

  1 = Disable FIFO. All read data transfers take place without the FIFO.

BST: Burst Mode Disable. Default after a software reset if LOCK is 0. If LOCK is 1, BST retains its value after a software reset.

Note: This bit is only valid if the FIFO is enabled in the Configure command. If the FIFO is not enabled in the Configure command, then this bit is a don't care.

- **0** = Burst mode enabled for FIFO Execution Phase data transfers. (default)

1 = Non-Burst mode enabled. The DRQ or IRQ pin is strobed once for each byte to be transferred while the FIFO is enabled.

R255: Recalibrate Step Pulses. The bit determines the maximum number of recalibrate step pulses the controller issues before terminating with an error. Default after a software reset.

- **0** = 85 maximum recalibrate step pulses. If ETR = 1, controller issues 3925 recalibrate step pulses maximum.

  1 = 255 maximum recalibrate step pulses. If ETR = 1, controller issues 4095 maximum recalibrate step pulses.

DENSEL: Density Select Pin Configuration. This two-bit value configures the Density Select output to one of three possible modes.

The default mode configures the DENSEL pin according to the state of bit 5 of the SuperI/O FDC Configuration register (offset 0xF0 from Logical Device 3) after a data rate has been selected. See Table 5-11.

If bit 5 of SuperI/O FDC Configuration register is high, the DENSEL pin is active high for the 500 Kbps or 1 Mbps data rates.

If bit 5 of the SuperI/O FDC Configuration register is low, the DENSEL pin is active low for the 500 Kbps or 1 Mbps data rates.

In addition to these modes, the DENSEL output signal can be set to always low or always high, as shown in Table 5-12. This provides more flexibility with new drive types.

TABLE 5-11. DENSEL Default Encoding

Data Rate	DENSEL (default)	
	SuperI/O FDC Configuration Register	
	Bit 5 = 1	Bit 5 = 0
250 Kbps	low	high
300 Kbps	low	high
500 Kbps	high	low
1 Mbps	high	low

TABLE 5-12. DENSEL Encoding

Mode Command		DENSEL Pin Definition
Bit 1	Bit 0	
0	0	Pin low
0	1	Pin high
1	0	Undefined
1	1	DEFAULT

BFR: CMOS Disk Interface Buffer Enable.

- **0** = Drive output signals configured as standard 4 mA push-pull outputs (actually 40 mA sink, 4 mA source). (default)

  1 = Drive output signals configured as 40 mA open-drain outputs.

WLD: Scan Wild Card.

- **0** = An FFh from either the µP or the disk during a Scan command is interpreted as a wild card character that always matches true. (default)

  1 = The Scan commands do not recognize FFh as a wild card character.

Head Settle: Time allowed for read/write head to settle after a seek during an Implied Seek operation.This is controlled as shown in Table 5-13, by loading a 4-bit value for N. (The default value for N is 8.)

TABLE 5-13. Head Settle Control

Data Rate (Kbps)	Multiplier 4 bits	Head Settle Time (msec)
250	N x 8	0 - 120
300	N x 6.666	0 - 100
500	N x 4	0 - 60
1000	N x 2	0 - 30

RG: Read Gate Diagnostic.

- **0** = Enable DSKCHG disk interface input for normal operation. (default)

  1 = Enable DSKCHG to act as an external Read Gate input signal to the Data Separator. This is intended as a test mode to aid in evaluation of the Data Separator.

NSC Command

The NSC command can be used to distinguish between the FDC versions and the 82077. The Result Phase byte uniquely identifies the floppy controller as a PC87308VUL, which returns a value of 73h. The 82077 and DP8473 return a value of 80h signifying an invalid command. The lower four bits of this result byte are subject to change by NSC, and reflects the particular version of the floppy disk controller part.

Perpendicular Mode Command

The Perpendicular Mode command is designed to support the unique Format and Write Data requirements of perpendicular (vertical) recording disk drives (4 Mbytes unformatted capacity). The Perpendicular Mode command configures each of the four logical drives as a perpendicular or conventional disk drive. Configuration of the four logical disk drives is done via the D3–D0 bits, or with the GAP and WG control bits. This command should be issued during the initialization of the floppy controller.

Perpendicular Recording drives operate in “Extra High Density” mode at 1 Mb/s, and are downward compatible with 1.44 Mbyte and 720 kbyte drives at 500 Kbps (High Density) and 250 Kbps (Double Density) respectively. If perpendicular drives are present in the system, this command should

be issued during initialization of the floppy controller, which configures each drive as perpendicular or conventional. Then, when a drive is accessed for a Format or Write Data command, the floppy controller adjusts the Format or Write Data parameters based on the data rate (*see* Table 5-14).

Looking at the second command byte, DC3-0 correspond to the four logical drives.

A 0 written to DCn sets drive n to conventional mode, and a 1 sets drive n to perpendicular mode. Also, the OW (Overwrite) bit offers additional control. When OW = 1, changing the values of DC3-0 (drive configuration bits) is enabled. When OW = 0, the internal values of DC3–0 are unaffected, regardless of what is written to DC3–0.

The function of the DCn bits must also be qualified by setting both WG and GAP to 0. If WG and GAP are used (i.e. not set to 00), they overrides whatever is programmed in the DCn bits. Table 5-14 indicates the operation of the FDC based on the values of GAP and WG. Note that when GAP and WG are both 0, the DCn bits are used to configure each logical drive as conventional or perpendicular. DC3-0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset. A hardware reset resets all the bits to zero (conventional mode for all drives). The Perpendicular Mode command bits may be rewritten at any time.

Note:

When in the Perpendicular Mode for any drive at any data rate selected by the DC3-0 bits, write precompensation is set to zero.

Perpendicular recording type disk drives have a pre-erase head which leads the read/write head by 200 µm, which translates to 38 bytes at the 1 Mbps data transfer rate (19 bytes at 500 Kbps). The increased spacing between the two heads requires a larger GAP2 between the Address Field and Data Field of a sector at 1 Mbps. (See Perpendicular Format in Figure 5-6.) This GAP2 length of 41 bytes (at 1 Mbps) ensures that the preamble in the Data Field is completely “pre-erased” by the Pre-Erase Head. Also, during Write Data operations to a perpendicular drive, a portion of GAP2 must be rewritten by the controller to guarantee that the Data Field Preamble has been pre-erased (see Table 5-14).

Read Data Command

The Read Data command reads logical sectors containing a Normal Data AM from the selected drive and makes the data available to the host µP. After the last Command Phase byte is written, the controller simulates the Motor On time for the selected drive internally. Turn on the drive motor directly by enabling the appropriate drive and motor select disk interface outputs with the Digital Output Register (DOR).

If Implied Seeks are enabled, the controller performs a Seek operation to the track number specified in the Command Phase. The controller also issues a Sense Interrupt for the seek and waits the Head Settle time specified in the Mode command.

The correct ID information (track, head, sector, bytes per sector) for the desired sector must be specified in the command bytes. See Table 5-16 Sector Size Selection for details on the bytes per sector code.

In addition, the End of Track Sector Number (EOT) should be specified, allowing the controller to read multiple sectors. The Data Length byte is a don't care and should be set to FFh.

TABLE 5-14. Effect of Drive Mode and Data Rate on Format and Write Commands

Data Rate	Drive Mode	GAP2 Length Written During Format	Portion of GAP2 Re-Written by Write Data Command
250/300/500 Kbps	Conventional Perpendicular	22 bytes 22 bytes	0 bytes 19 bytes
1 Mbps	Conventional Perpendicular	22 bytes 41 bytes	0 bytes 38 bytes

TABLE 5-15. Effect of GAP and WG on Format and Write Commands

GAP	WG	Mode Description	GAP2 Length Written During Format	Portion of GAP2 Re-Written by Write Data Command
0	0	Conventional	22 bytes	0 bytes
0	1	Perpendicular (500 Kbps)	22 bytes	19 bytes
1	0	Reserved (Conventional)	22 bytes	0 bytes
1	1	Perpendicular (1 Mbps)	41 bytes	38 bytes

TABLE 5-16. Sector Size Selection

Bytes per Sector Code	Bytes in Data Field
0	128
1	256
2	512
3	1024
4	2048
5	4096
6	8192
7	16384

The controller then starts the Data Separator and waits for the Data Separator to find the next sector Address Field. The controller compares the Address Field ID information (track, head, sector, bytes per sector) with the desired ID specified in the Command Phase. If the sector ID bytes do not match, then the controller waits for the Data Separator to find the next sector Address Field. The ID comparison process repeats until the Data Separator finds a sector Address Field ID that matches that in the command bytes, or until an error occurs. Possible errors are:

1. The µP aborted the command by writing to the FIFO. If there is no disk in the drive, the controller hangs up. The µP must then take the controller out of this hung state by writing a byte to the FIFO. This puts the controller into the Result Phase.
2. Two index pulses were detected since the search began, and no valid ID has been found. If the track address ID differs, the WT bit or BT bit (if the track address is FFh is set in ST2. If the head, sector, or bytes per sector code did not match, the ND bit is set in ST1. If the Address Field AM was never found, the MA bit is set in ST1.
3. The Address Field was found with a CRC error. The CE bit is set in ST1.

Once the desired sector Address Field is found, the controller waits for the Data Separator to find the subsequent Data Field for that sector. If the Data Field (normal or deleted) is not found with the expected time, the controller terminates the operation and enters the Result Phase (MD is set in ST2). If a Deleted Data Mark is found and SK was set in the Opcode command byte, the controller skips this sector and searches for the next sector Address Field as described above. The effect of SK on the Read Data command is summarized in Table 5-17.

Having found the Data Field, the controller then transfers data bytes from the disk drive to the host (described in Section 5.1.2 on page 52 Controller Phases) until the bytes per sector count has been reached, or the host terminates the operation (through TC, end of track, or implicitly through overrun). The controller then generates the CRC for the sector and compares this value with the CRC at the end of the Data Field.

Having finished reading the sector, the controller continues reading the next logical sector unless one or more of the following termination conditions occurred:

1. The DMA controller asserted TC. The IC bits in ST0 are set to Normal Termination.
2. The last sector address (of side 1 if MT was set) was equal to EOT. The EOT bit in ST1 is set. The IC bits in ST0 are set to Abnormal Termination. This is the expected condition during Non-DMA transfers.
3. Overrun error. The OR bit in ST1 is set. The IC bits in ST0 are set to Abnormal Termination. If the µP cannot service a transfer request in time, the last correctly read byte is transferred.
4. CRC error. CE bit in ST1, and CD bit in ST2, are set. The IC bits in ST0 are set to Abnormal Termination.

If MT was set in the Opcode command byte, and the last sector of side 0 has been transferred, the controller then continues with side 1.

Upon terminating the Execution Phase of the Read Data command, the controller asserts IRQ, indicating the beginning of the Result Phase. The µP must then read the result bytes from the FIFO. The values that are read back in the result bytes are shown in Table 5-19. If an error occurs, the result bytes indicate the sector read when the error occurred.

Read Deleted Data Command

The Read Deleted Data command reads logical sectors containing a Deleted Data AM from the selected drive and makes the data available to the host µP. This command is identical to the Read Data command, except for the setting of the CM bit in ST2 and the skipping of sectors. The effect of SK on the Read Deleted Data command is summarized in Table 5-18. See Table 5-19 for the state of the result bytes for a Normal Termination of the command.

Read ID Command

The Read ID command finds the next available Address Field and returns the ID bytes (track, head, sector, bytes per sector) to the µP in the Result Phase. There is no data transfer during the Execution Phase of this command. An interrupt is generated when the Execution Phase is completed.

The controller first simulates the Motor On time for the selected drive internally. The user must turn on the drive motor directly by enabling the appropriate drive and motor select disk interface outputs with the Digital Output Register (DOR). The Read ID command does not perform an implied seek.

After waiting the Motor On time, the controller starts the Data Separator and waits for the Data Separator to find the next sector Address Field. If an error condition occurs, the IC bits in ST0 are set to Abnormal Termination, and the controller enters the Result Phase. Possible errors are:

1. The µP aborted the command by writing to the FIFO. If there is no disk in the drive, the controller hangs up. The µP must then take the controller out of this hung state by writing a byte to the FIFO. This puts the controller into the Result Phase.
2. Two index pulses were detected since the search began, and no AM has been found. If the Address Field AM was never found, the MA bit is set in ST1.

TABLE 5-17. SK Effect on Read Data Command

SK	Data Type	Sector Read?	CM bit (ST2)	Description of Results
0	Normal	Y	0	Normal Termination
0	Deleted	Y	1	No Further Sectors Read
1	Normal	Y	0	Normal Termination
1	Deleted	N	1	Sector Skipped

TABLE 5-18. SK Effect on Read Deleted Data Command

SK	Data Type	Sector Read?	CM bit (ST2)	Description of Results
0	Normal	Y	1	No Further Sectors Read
0	Deleted	Y	0	Normal Termination
1	Normal	N	1	Sector Skipped
1	Deleted	Y	0	Normal Termination

TABLE 5-19. Result Phase Termination Values with No Error

MT	HD	Last Sector	ID Information at Result Phase			
			Track	Head	Sector	Bytes/Sector
0	0	< EOT	NC	NC	S + 1	NC
0	0	= EOT	T + 1	NC	1	NC
0	1	< EOT	NC	NC	S + 1	NC
0	1	= EOT	T + 1	NC	1	NC
1	0	< EOT	NC	NC	S + 1	NC
1	0	= EOT	NC	1	1	NC
1	1	< EOT	NC	NC	S + 1	NC
1	1	= EOT	T + 1	0	1	NC

EOT = End of Track Sector Number from Command Phase
S = Sector Number last operated on by controller
NC = No Change in Value
T = Track Number programmed in Command Phase

Read A Track Command

The Read a Track command reads sectors in physical order from the selected drive and makes the data available to the host. This command is similar to the Read Data command except for the following differences:

1. The controller waits for the index pulse before searching for a sector Address Field. If the µP writes to the FIFO before the index pulse, the command enters the Result Phase with the IC bits in ST0 set to Abnormal Termination.
2. A comparison of the sector Address Field ID bytes is performed, except for the sector number. The internal sector address is set to 1, and then incremented for each successive sector read.
3. If the Address Field ID comparison fails, the controller sets ND in ST1, but continues to read the sector. If there is a CRC error in the Address Field, the controller sets CE in ST1, but continues to read the sector.
4. Multi-track and Skip operations are not allowed. SK and MT should be set to 0.
5. If there is a CRC error in the Data Field, the controller sets CE in ST1 and CD in ST2, but continues reading sectors.
6. The controller reads a maximum of EOT physical sectors. There is no support for multi-track reads.

Recalibrate Command

The Recalibrate command is very similar to the Seek command. The controller sets the Present Track Register (PTR) of the selected drive to zero. It then steps the head of the selected drive out until the TRK0 disk interface input signal goes active, or until the maximum number of step pulses have been issued. See Table 5-20 for the maximum recalibrate step pulse values based on the R255 and ETR bits in the Mode command. If the number of tracks on the disk drive exceeds the maximum number of recalibrate step pulses, another Recalibrate command may need to be issued.

TABLE 5-20. Maximum Recalibrate Step Pulses Based on R255 and ETR

R255	ETR	Maximum Recalibrate Step Pulses
0	0	85 (default)
1	0	255
0	1	3925
1	1	4095

After the last command byte is issued, the DRx BUSY bit is set in the MSR for the selected drive. The controller simulates the Motor On time, and then enters the Idle Phase.

The execution of the actual step pulses occur while the controller is in the Drive Polling Phase. An interrupt is generated after the TRK0 signal is asserted, or after the maximum number of recalibrate step pulses are issued. There is no Result Phase. Recalibrates on more than one drive at a time should not be issued for the same reason as explained in the Seek command. No other command except the Sense Interrupt command should be issued while a Recalibrate command is in progress.

Relative Seek Command

The Relative Seek command steps the selected drive in or out a given number of steps. This command steps the read/write head an incremental number of tracks, as opposed to comparing against the internal present track register for that drive. The Relative Seek parameters are defined as follows:

DIR: Read/Write Head Step Direction Control

0 = Step Head Out

1 = Step Head In

RTN: Relative Track Number. This value determines how many incremental tracks to step the head in or out from the current track number.

The controller issues RTN number of step pulses and update the Present Track Register for the selected drive. The one exception to this is if the TRK0 disk input goes active, which indicates that the drive read/write head is at the outermost track. In this case, the step pulses for the Relative Seek are terminated, and the PTR value is set according to the actual number of step pulses issued. The arithmetic is done modulo 255. The DRx BUSY bit in the MSR is set for the selected drive. The controller simulates the Motor On time before issuing the step pulses. After the Motor On time, the controller enters the Idle Phase. The execution of the actual step pulses occurs in the Idle Phase of the controller.

After the step operation is complete, the controller generates an interrupt. There is no Result Phase. Relative Seeks on more than one drive at a time should not be issued for the same reason as explained in the Seek command. No other command except the Sense Interrupt command should be issued while a Relative Seek command is in progress.

Scan Commands

The Scan command allow data read from the disk to be compared against data sent from the µP. There are three Scan command to choose from:

Scan Equal	Disk Data = µP Data
Scan Low or Equal	Disk Data ≤ µP Data
Scan High or Equal	Disk Data ≥ µP Data

Each sector is interpreted with the most significant bytes first. If the Wildcard mode is enabled in the Mode command, an FFh from either the disk or the µP is used as a don't care byte that always matches equal. After each sector is read, if the desired condition has not been met, the next sector is read. The next sector is defined as the current sector number plus the Sector Step Size specified. The Scan command continues until the scan condition has been met, or the EOT has been reached, or if TC is asserted.

Read errors on the disk have the same error conditions as the Read Data command. If the SK bit is set, sectors with deleted data marks are ignored. If all sectors read are skipped, the command terminates with D3 of ST2 set (Scan Equal Hit). The Result Phase of the command is shown in Table 5-21.

TABLE 5-21. Scan Command Termination Values

Command	Status Register		Conditions
	D2	D3	
Scan Equal	0 1	1 0	Disk = µP Disk ≠ µP
Scan Low or Equal	0 0 1	1 0 0	Disk = µP Disk < µP Disk > µP
Scan High or Equal	0 0 1	1 0 0	Disk = µP Disk > µP Disk < µP

Seek Command

The Seek command issues step pulses to the selected drive in or out until the desired track number is reached. During the Execution Phase of the Seek command, the track number to seek to is compared with the present track number. The controller determines how many step pulses to issue and the DIR disk interface output indicates which direction the R/W head should move. The DRx BUSY bit is set in the MSR for the appropriate drive. The controller waits the Motor On time before issuing the first step pulse.

After the Motor On time, the controller enters the Idle Phase. The execution of the actual step pulses occurs in the Drive Polling phase of the controller. The step pulse rate is determined by the value programmed in the Specify command. An interrupt is generated one step pulse period after the last step pulse is issued. There is no Result Phase. A Sense Interrupt command should be issued to determine the cause of the interrupt.

While the internal micro-engine is capable of multiple seek on two or more drives at the same time, software should ensure that only one drive is seeking or recalibrating at a time. This is because the drives are actually selected via the DOR, which can only select one drive at a time. No other command except a Sense Interrupt command should be issued while a Seek command is in progress.

If the extended track range mode is enabled with the ETR bit in the Mode command, a fourth command byte should be written in the Command Phase to indicate the four most significant bits of the desired track number. Otherwise, only three command bytes should be written.

Sense Drive Status Command

The Sense Drive Status command returns the status of the selected disk drive in ST3. This command does not generate an interrupt.

Sense Interrupt Command

The Sense Interrupt command is used to determine the cause of interrupt when the interrupt is a result of the change in status of any disk drive. Four possible causes of the interrupt are:

1. Upon entering the Result Phase of:
   A. Read Data command
   B. Read Deleted Data command
   C. Read a Track command
   D. Read ID command
   E. Write Data command
   F. Write Deleted Data command
   G. Format command
   H. Scan command
   I. Verify command
2. During data transfers in the Execution Phase while in the Non-DMA mode.
3. Ready Changed State during the polling mode for an internally selected drive. (Occurs only after a hardware or software reset).
4. Seek, Relative Seek, or Recalibrate termination.

An interrupt due to reasons 1 and 2 does not require the Sense Interrupt command and is cleared automatically. This interrupt occurs during normal command operations and is easily discernible by the µP via the MSR. This interrupt is cleared reading or writing information from/to the Data Register (FIFO).

Interrupts caused by reasons 3 and 4 are identified with the aid of the Sense Interrupt command. The interrupt is cleared after the first result byte has been read. Use bits 5, 6, and 7 of ST0 to identify the cause of the interrupt as shown in Table 5-22.

Issuing a Sense Interrupt command without an interrupt pending is treated as an Invalid command. If the extended track range mode is enabled, a third byte should be read in the Result Phase, which indicate the four most significant bits of the present track number. Otherwise, only two result bytes should be read.

TABLE 5-22. Status Register 0 Termination Codes

Status Register 0			Cause
Interrupt Code		Seek End	
D7	D6	D5	
1	1	0	Internal Ready Went True
0	0	1	Normal Seek Termination
0	1	1	Abnormal Seek Termination

Set Track Command

This command is used to inspect or change the value of the internal Present Track Register. This could be useful for recovery from disk mis-tracking errors, where the real current track could be read through the Read ID command, and then the Set Track command could be used to set the internal Present Track Register to the correct value.

If the WNR bit is a 0, a track register is to be read. In this case, the Result Phase byte contains the value in the internal register specified, and the third byte in the Command Phase is a dummy byte.

If the WNR bit is a 1, data is written to a track register. In this case the third byte of the Command Phase is written to the specified internal track register, and the Result Phase byte contains this new value.

The DS1 and DS0 bits select the Present Track Register for the particular drive. The internal register address depends on MSB, DS1 and DS0 as shown in Table 5-23. This command does not generate an interrupt

TABLE 5-23. Set Track Register Address

DS1	DS0	MSB	Register Addressed
0	0	0	PTR0 (LSB)
0	0	1	PTR0 (MSB)
0	1	0	PTR1 (LSB)
0	1	1	PTR1 (MSB)
1	0	0	PTR2 (LSB)
1	0	1	PTR2 (MSB)
1	1	0	PTR3 (LSB)
1	1	1	PTR3 (MSB)

Specify Command

The Specify command sets the initial values for three internal timers. The function of these Specify parameters is described below. The parameters of this command are undefined after power up, and are unaffected by any reset. Thus, software should always issue a Specify command as part of an initialization routine. This command does not generate an interrupt.

The Motor Off and Motor On timers are artifacts of the µPD765. These timers determine the delay from selecting a drive motor until a read or write operation is started, and the delay of deselecting the drive motor after the command is completed. Since the FDC enables the drive and motor select line directly through the DOR, these timers only provide some delay from the initiation of a command until it is actually started.

Step Rate Time: These four bits define the time interval between successive step pulses during a seek, implied seek, recalibrate, or relative seek. The programming of this step rate is shown in Table 5-24.

TABLE 5-24. Step Rate Time (SRT) Values

Data Rate	Value	Range	Units
1 Mb/s	(16 - SRT)/2	0.5 - 8	ms
500 Kbps	(16 - SRT)	1 - 16	ms
300 Kbps	(16 - SRT) x 1.67	1.67 - 26.7	ms
250 Kbps	(16 - SRT) x 2	2 - 32	ms

Motor Off Time: These four bits determine the simulated Motor Off time as shown in Table 5-25.

Motor On Time: These seven bits determine the simulated Motor On time as shown in Table 5-26.

DMA: This bit selects the data transfer mode in the Execution Phase of a read, write, or scan operation.

0 = DMA mode is selected.

1 = Non-DMA mode is selected.

Verify Command

The Verify command reads logical sectors containing a Normal Data AM from the selected drive without transferring the data to the host. This command is identical to the Read Data command, except that no data is transferred during the Execution Phase.

The Verify command is designed for post-format or post-write verification. Data is read from the disk, as the controller checks for valid Address Marks in the Address and Data Fields. The CRC is computed and checked against the previously stored value on the disk. The EOT value should be set to the final sector to be checked on each side. If EOT is greater than the number of sectors per side, the command terminates with an error and no useful Address Mark or CRC data is given.

The TC pin cannot be used to terminate this command since no data is transferred. The command can simulate a TC by setting the EC bit to a 1. In this case, the command terminates when SC (Sector Count) sectors have been read. (If SC = 0 then 256 sectors is verified). If EC = 0, then the command terminates when EOT is equal to the last sector to be checked. In this case, the Data Length parameter should be set to FFh. Refer to Table 5-19 for the Result Phase values for a successful completion of the command. Also see Table 5-27 for further explanation of the result bytes with respect to the MT and EC bits.

Version Command

The Version command can be used to determine the floppy controller being used. The Result Phase uniquely identifies the floppy controller version. The FDC returns a value of 90h in order to be compatible with the 82077. The DP8473 and other NEC765 compatible controllers return a value of 80h (invalid command).

Write Data Command

The Write Data command receives data from the host and writes logical sectors containing a Normal Data AM to the selected drive. The operation of this command is similar to the Read Data command except that the data is transferred from the µP to the controller instead of the other way around.

The controller simulates the Motor On time before starting the operation. If implied seeks are enabled, the seek and sense interrupt functions are then performed. The controller then starts the Data Separator and waits for the Data Separator to find the next sector Address Field.

The controller compares the Address ID (track, head, sector, bytes per sector) with the desired ID specified in the Command Phase. If there is no match, the controller waits to find the next sector Address Field.

This process continues until the desired sector is found. If an error condition occurs, the IC bits in ST0 are set to Abnormal Termination, and the controller enters the Result Phase. Possible errors are:

1. The µP aborted the command by writing to the FIFO. If there is no disk in the drive, the controller hangs up. The µP must then take the controller out of this hung state by writing a byte to the FIFO. This puts the controller into the Result Phase.

2. Two index pulses were detected since the search began, and no valid ID has been found. If the track address ID differs, the WT bit or BT bit (if the track address is FFh) is set in ST2. If the head, sector, or bytes per sector code did not match, the ND bit is set in ST1. If the Address Field AM was never found, the MA bit is set in ST1.
3. The Address Field was found with a CRC error. The CE bit is set in ST1.
4. If the controller detects the Write Protect disk interface input is asserted, bit 1 of ST1 is set.

If the correct Address Field is found, the controller waits for all (conventional mode) or part (perpendicular mode) of GAP2 to pass. The controller then writes the preamble field, address marks, and data bytes to the Data Field. The data bytes are transferred to the controller by the µP.

Having finished writing the sector, the controller continues reading the next logical sector unless one or more of the following termination conditions occurred:

1. The DMA controller asserted TC. The IC bits in ST0 are set to Normal Termination.
2. The last sector address (of side 1 if MT was set) was equal to EOT. The EOT bit in ST1 is set. The IC bits in ST0 are set to Abnormal Termination. This is the expected condition during Non-DMA transfers.
3. Underrun error. The OR bit in ST1 is set. The IC bits in ST0 are set to Abnormal Termination. If the µP cannot service a transfer request in time, the last correctly written byte is written to the disk.

If MT was set in the Opcode command byte, and the last sector of side 0 has been transferred, the controller then continues with side 1.

Write Deleted Data

The Write Deleted Data command receives data from the host and writes logical sectors containing a Deleted Data AM to the selected drive. This command is identical to the Write Data command except that a Deleted Data AM is written to the Data Field instead of a Normal Data AM.

TABLE 5-25. Motor Off Time (MFT) Values

Data Rate	Mode 1 (TMR = 0)		Mode 2 (TMR = 1)		Units
	Value	Range	Value	Range	
1 Mbps	MFT x 8	8-128	MFT x 512	512-8192	msec
500 Kbps	MFT x 16	16-256	MFT x 512	512-8192	msec
300 Kbps	MFT x 80/3	26.7-427	MFT x 2560/3	853-13653	msec
250 Kbps	MFT x 32	32-512	MFT x 1024	1024-16384	msec

Note: Motor Off Time = 0 is treated as MFT = 16.

TABLE 5-26. Motor On Time (MNT) Values

Data Rate	Mode 1 (TMR = 0)		Mode 2 (TMR = 1)		Units
	Value	Range	Value	Range	
1 Mbps	MNT	1-128	MNT x 32	32-4096	msec
500 Kbps	MNT	1-128	MNT x 32	32-4096	msec
300 Kbps	MNT x 10/3	3.3-427	MNT x 160/3	53-6827	msec
250 Kbps	MNT x 4	4-512	MNT x 64	64-8192	msec

Note: Motor On Time = 0 is treated as MNT = 128

TABLE 5-27. Verify Command Result Phase Table

MT	EC	Sector Count (SC) / End of Track (EOT) Value	Termination Result
0	0	DTL used (should be FFh) EOT ≤ Number of Sectors per Side	No Errors
0	0	DTL used (should be FFh) EOT > Number of Sectors per Side	Abnormal Termination
0	1	SC ≤ Number of Sectors per Side AND SC ≤ EOT	No Errors
0	1	SC > Number of Sectors Remaining OR SC > EOT	Abnormal Termination
1	0	DTL used (should be FFh) EOT ≤ Number of Sectors per Side	No Errors
1	0	DTL used (should be FFh) EOT > Number of Sectors per Side	Abnormal Termination
1	1	SC ≤ Number of Sectors per Side AND SC ≤ EOT	No Errors
1	1	SC ≤ (EOT x 2) AND EOT ≤ Number of Sectors per Side	No Errors
1	1	SC > (EOT x 2)	Abnormal Termination

Notes:

1. Number of Sectors per Side = number of formatted sectors per each side of the disk.
2. Number of Sectors Remaining = number of formatted sectors left which can be read, which includes side 1 of the disk if the MT bit is set to 1.
3. If MT = 1 and the SC value is greater that the number of remaining formatted sectors on side 0, verifying continues on side 1 of the disk.

6.0 Parallel Port (Logical Device 4)

The Parallel Port is a communications device that transfers parallel data between the system and an external device. Originally designed to output data to an external printer, the use of this port has grown to include bidirectional communications, increased data rates and additional applications (such as network adaptors).

6.1 PARALLEL PORT CONFIGURATION

The PC87308VUL Parallel Port device offers a wide range of operational configurations. It utilizes the most advanced protocols in current use, while maintaining full backward compatability to support existing hardware and software. It supports two Standard Parallel Port (SPP) modes of operation for parallel printer ports (as found in the IBM PC-AT, PS/2 and Centronics systems), two Enhanced Parallel Port (EPP) modes of operation, and one Extended Capabilities Port (ECP) mode. This versatility is achieved by user software control of the mode in which the device functions.

The IEEE 1284 standard establishes a widely accepted handshake and transfer protocol that ensures transfer data integrity. This parallel interface fully supports the IEEE 1284 standard of parallel communications, in both Legacy and Plug and Play configurations, in all modes except the EPP revision 1.7 mode described in the next section.

6.1.1 Parallel Port Operation Modes

The PC87308VUL parallel port supports Standard Parallel Port (SPP), Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP) configurations.

- In the Standard Parallel Port (SPP) configuration, data rates of several hundred bytes per second are achieved. This configuration supports the following operation modes:
  - — In SPP Compatible mode the port is write-only (for data). Data transfers are software-controlled and are accompanied by status and control handshake signals.
  - — PP FIFO mode is the same as SPP Compatible mode with the addition of an output data FIFO, and operates as a state-machine instead of software-controlled operation.
  - — In SPP Extended mode, the parallel port becomes a read/write port, that can transfer a full data byte in either direction.
- The Enhanced Parallel Port (EPP) configuration supports two modes that offer higher bi-directional throughput and more efficient hardware-based handling.
  - — The EPP revision 1.7 mode lacks a comprehensive handshaking scheme to ensure data transfer integrity between communicating devices with dissimilar data rates. This is the only mode that does not meet the requirements of the IEEE 1284 standard handshake and transfer protocol.
  - — EPP revision 1.9 mode offers data transfer enhancement, while meeting the IEEE 1284 standard.
- The Extended Capabilities Port (ECP) configuration extends the port capabilities beyond EPP modes by adding a bi-directional 16-level FIFO with threshold interrupts, for PIO and DMA data transfer, including demand DMA operation. In this mode, the device becomes a hardware state-machine with highly efficient data transfer control by hardware in real-time.

  The PC87308VUL enters the ECO mode by default after reset.

  The ECP configuration supports several modes that are determined by bits 7-5 of the ECP Extended Control Register (ECR) at offset 402h. Section 6.6 on page 101 describes these modes in detail. The ECR register is described in Section 6.5.12 on page 97.

6.1.2 Configuring Operation Modes

The operation mode of the parallel port is determined by configuration bits that are controlled by software. If ECP mode is set upon initial system configuration, the operation mode may also be changed during run-time.

- **Configuration at System Initialization (Static)** - The parallel port operation mode is determined at initial system configuration by bits 7-4 of the SuperI/O Parallel Port Configuration register at index F0h of logical device 4. See Section 2.7.1 on page 24.
- **Configuration at System Initialization with Run-Time Reconfiguration (Dynamic)** - The parallel port operation mode is initially ECP, but may be changed by additional mode selection bits if bit 4 of the SuperI/O Parallel Port Configuration register at index F0h of logical device 4 is 1, and bits 7-5 of the same register are 110 or 111.

  In this case, the operation mode is determined by bits 7-5 of the parallel port Extended Control register (ECR) at parallel port base address + 402h and by bits 7 and 4 of the Control2 register at second level offset 2. These registers are accessed via the internal ECP Mode Index and Data registers at parallel port base address + 403 and parallel port base address + 404h, respectively.

Table 6-1 shows how to configure the parallel port for the different operation modes.

Table 2-4 on page 13 shows how to allocate a range for the base address of the parallel port for each mode. Parallel port address decoding is described in Chapter 2.2.2 on page 12.

The parallel port supports Plug and Play operation. Its interrupt can be routed on one of the following ISA interrupts: IRQ1 to IRQ15 except for IRQ 2 and 13. Its DMA signals can be routed to one of three 8-bit ISA DMA channels. See Section 6.5.19 on page 100.

The parallel port device is activated by setting bit 4 of the system Function Enable Register 1 (FER1) to 1. See Section 9.2.3 on page 158.

6.1.3 Output Pin Protection

The parallel port output pins are protected against potential damage from connecting an unpowered port to a powered-up printer.

6.2 STANDARD PARALLEL PORT (SPP) MODES

Compatible SPP mode is a data write-only mode that outputs data to a parallel printer, using handshake bits, under software control.

In SPP Extended mode, parallel data transfer is bi-directional. Table 6-12 on page 107 lists the output signals for the standard 25-pin, D-type connector. Table 6-2 lists the reset states for handshake output pins in this mode.

TABLE 6-1. Parallel Port Mode Selection

Configuration Time	Operation Mode	SuperI/O Parallel Port Configuration Register (Index F0h)[a]	Extended Control Register (ECR) of the Parallel Port (Offset 402h) [b]	Control2 Register of the Parallel Port (Offset 02h) [c]	Notes
		7 6 5	7 6 5	4	
Configuration at System Initialization (Static)	SPP Compatible	0 0 0	-	-	-
	SPP Extended	0 0 1	-	-	-
	EPP Revision 1.7	0 1 0	-	-	-
	EPP Revision 1.9	0 1 1	-	-	-
Configuration at System Initialization with Run-Time Reconfiguration (Dynamic)	SPP Compatible	1 0 0 or 1 1 1	0 0 0	-	d
	PP FIFO		0 1 0	-	d
	SPP Extended		0 0 1	-	d
	EPP Revision 1.7	1 1 1	1 0 0	0	d
	EPP Revision 1.9			1	d
	ECP(Default)	1 0 0 or 1 1 1	0 1 1	-	-

a. Section 2.7.1 on page 24 describes the bits of the SuperI/O Parallel Port configuration register.
b. See Section 6.5.12 on page 97
c. Before modifying this bit, set bit 4 of the SuperI/O Parallel Port configuration register at index F0h to 1.
d. Use bit 7 of the Control2 register at second level offset 2 of the parallel port to further specify compatibility. See Section 6.5.17 on page 99.

TABLE 6-2. Parallel Port Reset States

Signal	Reset Control	State After Reset
SLIN	MR	TRI-STATE
INIT	MR	Zero
$\overline{AFD}$	MR	TRI-STATE
STB	MR	TRI-STATE
IRQ5,7	MR	TRI-STATE

6.2.1 Standard Parallel Port (SPP) Modes Register Set

In all Standard Parallel Port (SPP) modes, port operation is controlled by the registers listed in Table 6-3.

All register bit assignments are compatible with the assignments in existing SPP devices.

A single Data Register DTR is used for data input and output (see Section 6.2.2). The direction of data flow is determined by the system setting in bit 5 of the Control Register CTR.

TABLE 6-3. Standard Parallel Port (SPP) Registers

Offset	Name	Description	R/W
00h	DTR	Data	R/W
01h	STR	Status	R
02h	CTR	Control	R/W
03h		-	TRI-STATE

6.2.2 SPP Data Register (DTR), Offset 00h

This bidirectional data port transfers 8-bit data in the direction determined by bit 5 of SPP register CTR at offset 02h and mode.

The read or write operation is activated by the system $\overline{RD}$ and $\overline{WR}$ strobes.

Table 6-4 tabulates DTR register operation.

TABLE 6-4. SPP DTR Register Read and Write Modes

Mode	Bit 5 of CTR	$\overline{RD}$	$\overline{WR}$	Result
SPP Compatible	x	1	0	Data written to PD7-0.
	x	0	1	Data read from the output latch
SPP Extended	0	1	0	Data written to PD7-0.
	1	1	0	Data written is latched
	0	0	1	Data read from output latch.
	1	0	1	Data read from PD7-0.

In SPP Compatible mode, the parallel port does not write data to the output signals. Bit 5 of the CTR register has no effect in this state. If data is written ($\overline{WR}$ goes low), the data is sent to the output signals PD7-0. If a read cycle is initiated ($\overline{RD}$ goes low), the system reads the contents of the output latch, and not data from the PD7-0 output signals.

In SPP Extended mode, the parallel port can read and write external data via PD7-0. In this mode, bit 5 sets the direction for data in or data out, while read or write cycles are possible in both settings of bit 5.

If bit 5 of CTR is cleared to 0, data is written to the output signals PD7-0 when a write cycle occurs. (if a read cycle occurs in this setting, the system reads the output latch, not data from PD7-0).

If bit 5 of CTR is set to 1, data is read from the output signals PD7-0 when a read cycle occurs. A write cycle in this setting only writes to the output latch, not to the output signals PD7-0.

The reset value of this register is 0.

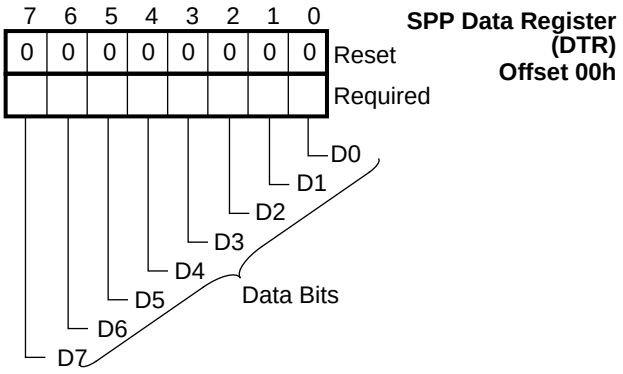


FIGURE 6-1. DTR Register Bitmap (SPP Mode)

6.2.3 Status Register (STR), Offset 01h

This read-only register holds status information. A system write operation to STR is an invalid operation that has no effect on the parallel port.

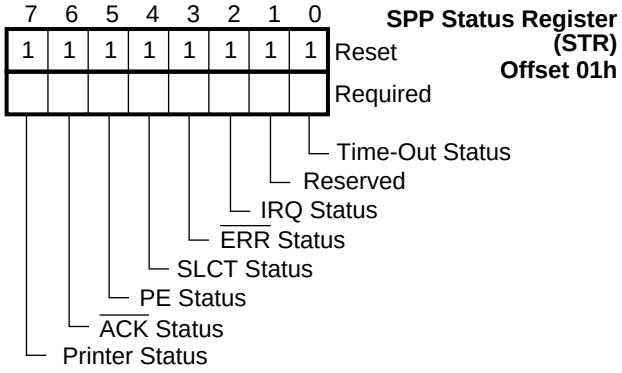


FIGURE 6-2. STR Register Bitmap (SPP Mode)

Bit 0 - Time-Out Status

In EPP modes only, this is the time-out status bit. In all other modes this bit has no function and has the constant value 1.

This bit is cleared when an EPP mode is enabled. Thereafter, this bit is set to 1 when a time-out occurs in an EPP cycle and is cleared when STR is read.

In EPP modes:

0 - An EPP mode is set. No time-out occurred since STR was last read.

1 - Time-out occurred on EPP cycle (minimum of 10 µsec). (Default)

Bit 1 - Reserved

This bit is reserved and is always 1.

Bit 2 - IRQ Status

In all modes except SPP Extended, this bit is always 1.

In SPP Extended mode this bit is the IRQ status bit. It remains high unless the interrupt request is enabled (bit 4 of CTR set high). This bit is high except when latched low when the $\overline{ACK}$ signal makes a low to high transition, indicating a character is now being transferred to the printer.

Reading this bit resets it to 1.

0 - Interrupt requested in SPP Extended mode.

1 - No interrupt requested. (Default)

Bit 3 - $\overline{ERR}$ Status

This bit reflects the current state of the printer error signal, $\overline{ERR}$. The printer sets this bit low when there is a printer error.

0 - Printer error.

1 - No printer error.

Bit 4 - SLCT Status

This bit reflects the current state of the printer select signal, SLCT. The printer sets this bit high when it is on-line and selected.

0 - No printer selected.

1 - Printer selected and online.

Bit 5 - PE Status

This bit reflects the current state of the printer paper end signal (PE). The printer sets this bit high when it detects the end of the paper.

0 - Printer has paper.

1 - End of paper in printer.

Bit 6 - $\overline{\text{ACK}}$ Status

This bit reflects the current state of the printer acknowledge signal, $\overline{\text{ACK}}$. The printer pulses this signal low after it has received a character and is ready to receive another one. This bit follows the state of the $\overline{\text{ACK}}$ pin.

0 - Character reception complete.

1 - No character received .

Bit 7 - Printer Status

This bit reflects the current state of the printer BUSY signal. The printer sets this bit low when it is busy and cannot accept another character.

This bit is the inverse of the (BUSY/$\overline{\text{WAIT}}$) pin.

0 - Printer busy.

1 - Printer not busy.

6.2.4 SPP Control Register (CTR), Offset 02h

The control register provides all the output signals that control the printer. Except for bit 5, it is a read and write register.

Normally when the Control Register (CTR) is read, the bit values are provided by the internal output data latch. These bit values can be superseded by the logic level of the $\overline{\text{STB}}$, $\overline{\text{AFD}}$, $\overline{\text{INIT}}$, and $\overline{\text{SLIN}}$ signals, if these signals are forced high or low by external voltage. To force these signals high or low the corresponding bits should be set to their inactive states (e.g., $\overline{\text{AFD}}$, $\overline{\text{STB}}$ and $\overline{\text{SLIN}}$ should all be 0; $\overline{\text{INIT}}$ should be 1).

Section 6.3.10 describes the transfer operations that are possible in EPP modes.

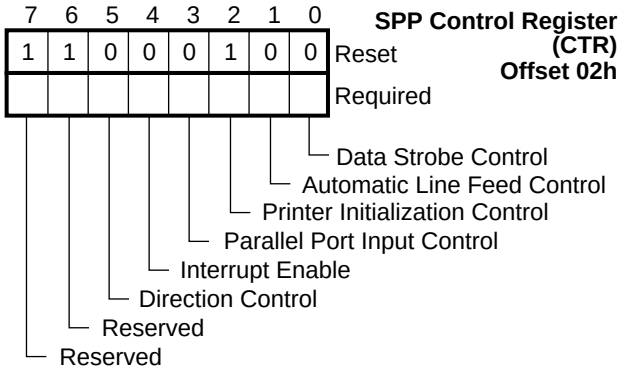


FIGURE 6-3. CTR Register Bitmap (SPP Mode)

Bit 0 - Data Strobe Control

Bit 0 directly controls the data strobe signal to the printer via the $\overline{\text{STB}}$ signal.

This bit is the inverse of the $\overline{\text{STB}}$ signal.

Bit 1 - Automatic Line Feed Control

This bit directly controls the automatic line feed signal to the printer via the $\overline{\text{AFD}}$ pin. Setting this bit high causes the printer to automatically feed after each line is printed.

This bit is the inverse of the $\overline{\text{AFD}}$ signal.

0 - No automatic line feed. (Default)

1 - Automatic line feed

Bit 2 - Printer Initialization Control

This bit directly controls the signal to initialize the printer via the $\overline{\text{INIT}}$ pin. Setting this bit to low initializes the printer.

The value of the $\overline{\text{INIT}}$ signal reflects the value of this bit.

The default setting of 1 on this bit prevents printer initialization in SPP mode, and enables ECP mode after reset.

0 - Initialize Printer.

1 - No action (Default).

Bit 3 - Select Input Signal Control

This bit directly controls the select in signal to the printer via the $\overline{\text{SLIN}}$ signal. Setting this bit high selects the printer.

It is the inverse of the $\overline{\text{SLIN}}$ signal.

This bit must be set to 0 before enabling the EPP or ECP mode.

0 - Printer not selected. (Default)

1 - Printer selected and online.

Bit 4 - Interrupt Enable

Bit 4 controls the interrupt generated by the $\overline{\text{ACK}}$ signal. Its function changes slightly depending on the parallel port mode selected.

In ECP mode, this bit should be set to 0.

In the following description, IRQx indicates an interrupt allocated for the parallel port.

0 - In SPP Compatible, SPP Extended and EPP modes, IRQx is floated. (Default)

1 - In SPP Compatible mode, IRQx follows $\overline{\text{ACK}}$ transitions.

In SPP Extended mode, IRQx is set active on the trailing edge of $\overline{\text{ACK}}$.

In EPP modes, IRQx follows $\overline{\text{ACK}}$ transitions, or is set when an EPP time-out occurs.

Bit 5 - Direction Control

This bit determines the direction of the parallel port in SPP Extended mode only. In the (default) SPP Compatible mode, this bit has no effect, since the port functions for output only.

This is a read/write bit in EPP modes. In SPP modes it is a write only bit. A read from it returns 1.

In SPP Compatible mode and in EPP modes it does not control the direction. See Table 6-4.

0 - Data output to PD7-0 in SPP Extended mode during write cycles. (Default)

1- Data input from PD7-0 in SPP Extended mode during read cycles.

Bits 7,6 - Reserved

These bits are reserved and are always 1.

6.3 ENHANCED PARALLEL PORT (EPP) MODES

EPP modes allow greater throughput than SPP modes by supporting faster transfer times (8, 16 or 32-bit data transfers in a single read or write operation) and a mechanism that allows the system to address peripheral device registers directly. Faster transfers are achieved by automatically generating the address and data strobes.

The connector pin assignments for these modes are listed in Table 6-12 on page 107.

EPP modes support revision 1.7 and revision 1.9 of the IEEE 1284 standard, as shown in Table 6-1.

In Legacy mode, EPP modes are supported for a parallel port whose base address is 278h or 378h, but not for a parallel port whose base address is 3BCh. (There are no EPP registers at 3BFh.) In both Legacy and Plug and Play modes, bits 2, 1 and 0 of the parallel port base address must be 000 in EPP modes.

SPP-type data transactions may be conducted in EPP modes. The appropriate registers are available for this type of transaction. (See Table 6-5.) As in the SPP modes, software must generate the control signals required to send or receive data.

6.3.1 Enhanced Parallel Port (EPP) Register Set

Table 6-5 lists the EPP registers. All are single-byte registers.

Bits 0, 1 and 3 of the CTR register must be 0 before the EPP registers can be accessed, since the signals controlled by these bits are controlled by hardware during EPP accesses. Once these bits are set to 0 by the software driver, multiple EPP access cycles may be invoked.

When EPP modes are enabled, the software can perform SPP Extended mode cycles. In other words, if there is no access to one of the EPP registers, EPP Address (ADDR) or EPP Data Registers 0-3 (DATA0-3), EPP modes behave like SPP Extended mode, except for the interrupt, which is pulse triggered instead of level triggered.

Bit 7 of STR ($\overline{\text{BUSY}}$ status) must be set to 1 before writing to DTR in EPP modes to ensure data output to PD7-0.

The enhanced parallel port monitors the IOCHRDY signal during EPP cycles. If IOCHRDY is driven low for more then 10 µsec, an EPP time-out event occurs, which aborts the cycle by asserting IOCHRDY, thus releasing the system from a stuck EPP peripheral device. (This time-out event is only functional when the clock is applied to this logical device).

When the cycle is aborted, $\overline{\text{ASTRB}}$ or $\overline{\text{DSTRB}}$ becomes inactive, and the time-out event is signaled by asserting bit 0 of STR. If bit 4 of CTR is 1, the time-out event also pulses the IRQ5 or IRQ7 signals when enabled. (IRQ5 and IRQ7 can be routed to any other IRQ lines via the Plug and Play block).

EPP cycles to the external device are activated by invoking read or write cycles to the EPP.

TABLE 6-5. Enhanced Parallel Port (EPP) Registers

Offset	Name	Description	Mode	R/W
00h	DTR	SPP Data	SPP or EPP	R/W
01h	STR	SPP Status	SPP or EPP	R
02h	CTR	SPP Control	SPP or EPP	R/W
03h	ADDR	EPP Address	EPP	R/W
04h	DATA0	EPP Data Port 0	EPP	R/W
05h	DATA1	EPP Data Port 1	EPP	R/W
06h	DATA2	EPP Data Port 2	EPP	R/W
07h	DATA3	EPP Data Port 3	EPP	R/W

6.3.2 SPP or EPP Data Register (DTR), Offset 00h

The DTR register is the SPP Compatible or SPP Extended data register. A write to DTR sets the state of the eight data pins on the 25-pin D-shell connector.

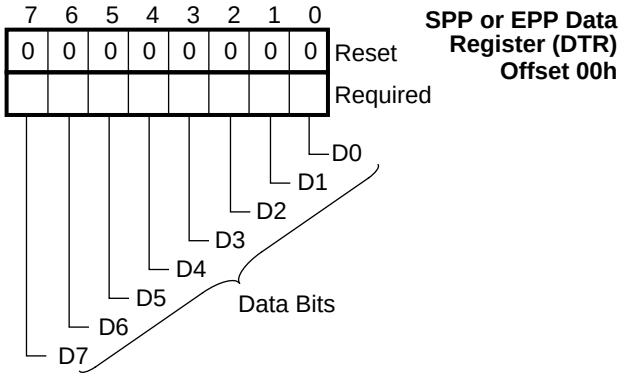


FIGURE 6-4. SPP or EPP DTR Register Bitmap

6.3.3 SPP or EPP Status Register (STR), Offset 01h

This status port is read only. A read presents the current status of the five pins on the 25-pin D-shell connector, and the IRQ as shown in Figure 6-5.

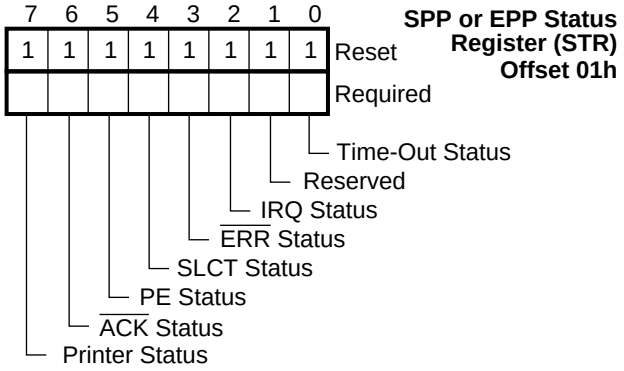


FIGURE 6-5. SPP or EPP STR Register Bitmap

The bits of this register have the identical function in EPP mode as in SPP mode. See Section 6.2.3 for a detailed description of each bit.

6.3.4 SPP or EPP Control Register (CTR), Offset 02h

This control port is read or write. A write operation to it sets the state of four pins on the 25-pin D-shell connector, and controls both the parallel port interrupt enable and direction.

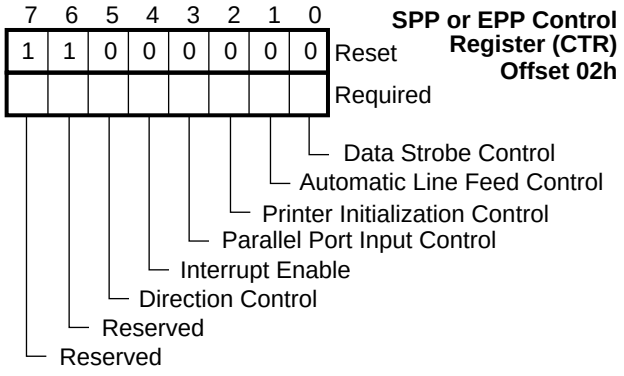


FIGURE 6-6. SPP or EPP CTR Register Bitmap

The bits of this register have the identical function in EPP modes as in SPP modes. See Section 6.2.4 for a detailed description of each bit.

6.3.5 EPP Address Register (ADDR), Offset 03h

This port is added in EPP modes to enhance system throughput by enabling registers in the remote device to be directly addressed by hardware.

This port can be read or written. Writing to it initiates an EPP device or register selection operation.

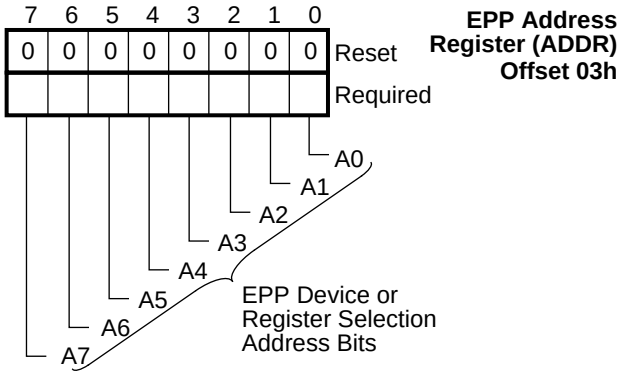


FIGURE 6-7. EPP ADDR Register Bitmap

6.3.6 EPP Data Register 0 (DATA0), Offset 04h

DATA0 is a read/write register. Accessing it initiates device read or write operations of bits 7 through 0.

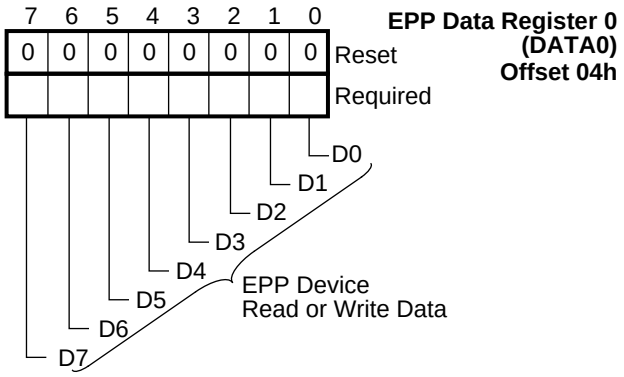


FIGURE 6-8. EPP DATA0 Register Bitmap

6.3.7 EPP Data Register 1 (DATA1), Offset 05h

DATA2 is only accessed to transfer bits 15 through 8 of a 16-bit read or write to EPP Data Register 0 (DATA0).

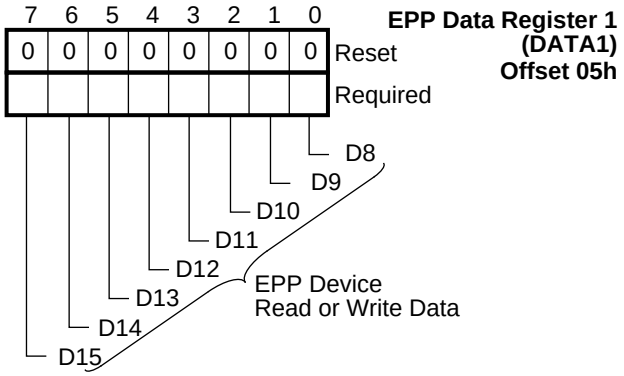


FIGURE 6-9. EPP DATA1 Register Bitmap

6.3.8 EPP Data Register 2 (DATA2), Offset 06h

This is the third EPP data register. It is only accessed to transfer bits 16 through 23 of a 32-bit read or write to EPP Data Register 0 (DATA0).

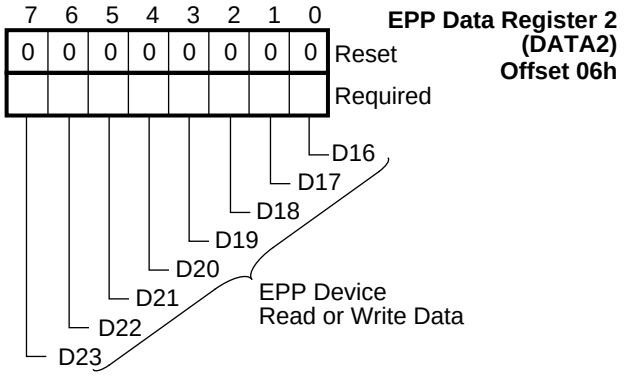


FIGURE 6-10. EPP DATA2 Register Bitmap

6.3.9 EPP Data Register 3 (DATA3), Offset 07h

This is the fourth EPP data register. It is only accessed to transfer bits 24 through 31 of a 32-bit read or write to EPP Data Register 0 (DATA0).

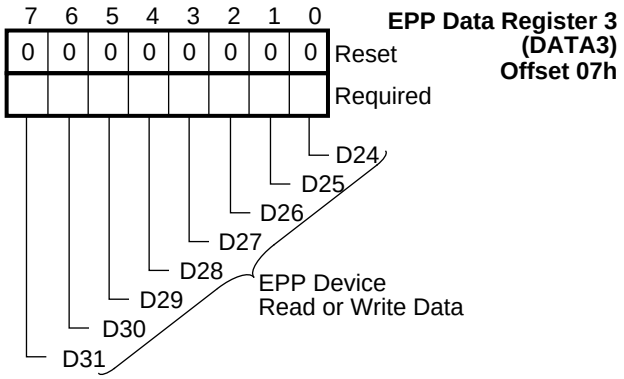


FIGURE 6-11. EPP DATA3 Register Bitmap

6.3.10 EPP Mode Transfer Operations

The EPP transfer operations are address read or write, and data read or write. An EPP transfer is composed of a system read or write cycle from or to an EPP register, and an EPP read or write cycle from a peripheral device to an EPP register or from an EPP register to a peripheral device.

EPP 1.7 Address Write

The following procedure selects a peripheral device or register as illustrated in Figure 6-12.

1. The system writes a byte to the EPP Address register. $\overline{WR}$ becomes low to latch D7-0 into the EPP Address register. The latch drives the EPP Address register onto PD7-0 and the EPP pulls $\overline{WRITE}$ low.
2. The EPP pulls $\overline{ASTRB}$ low to indicate that data was sent.
3. If $\overline{WAIT}$ was low during the system write cycle, IOCHRDY becomes low. When $\overline{WAIT}$ becomes high, the EPP pulls IOCHRDY high.
4. When IOCHRDY becomes high, it causes $\overline{WR}$ to become high. If $\overline{WAIT}$ is high during the system write cycle, then the EPP does not pull IOCHRDY to low.
5. When $\overline{WR}$ becomes high, it causes the EPP to pull first $\overline{ASTRB}$ and then $\overline{WRITE}$ to high. The EPP can change PD7-0 only when $\overline{WRITE}$ and $\overline{ASTRB}$ are both high.

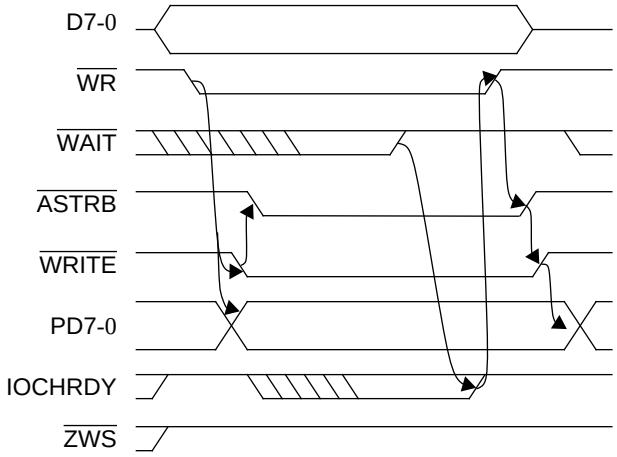


FIGURE 6-12. EPP 1.7 Address Write

EPP 1.7 Address Read

The following procedure reads from the EPP Address register as shown in Figure 6-13.

1. The system reads a byte from the EPP Address register. $\overline{RD}$ goes low to gate PD7-0 into D7-0.
2. The EPP pulls $\overline{ASTRB}$ low to signal the peripheral to start sending data.
3. If $\overline{WAIT}$ is low during the system read cycle. Then the EPP pulls IOCHRDY low. When $\overline{WAIT}$ becomes high, the EPP stops pulling IOCHRDY to low.
4. When IOCHRDY becomes high, it causes $\overline{RD}$ to become high. If $\overline{WAIT}$ is high during the system read cycle then the EPP does not pull IOCHRDY to low.
5. When $\overline{RD}$ becomes high, it causes the EPP to pull $\overline{ASTRB}$ high. The EPP can change PD7-0 only when $\overline{ASTRB}$ is high. After $\overline{ASTRB}$ becomes high, the EPP puts D7-0 in TRI-STATE.

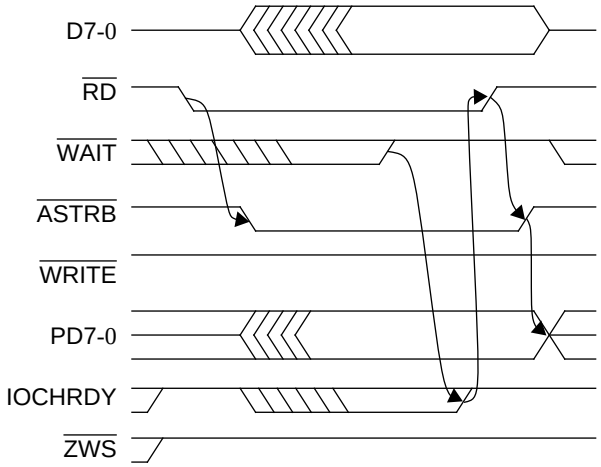


FIGURE 6-13. EPP 1.7 Address Read

EPP 1.7 Data Write and Read

This procedure writes to the selected peripheral device or register.

EPP 1.7 data read or write operations are similar to EPP 1.7 Address register read or write operations, except that the data strobe (DSTRB signal), and the EPP Data register, replace the address strobe (ASTRB signal) and the EPP Address register, respectively.

EPP Revision 1.7 and 1.9 Zero Wait State (ZWS) Address Write and Read Operations

The following procedure performs a short write to the selected peripheral device or register. See also Figure 6-14.

1. The system writes a byte to the EPP Address register. WR becomes low to latch D7-0 into the EPP Data register. The latch drives the EPP Data register to PD7-0.
2. The EPP first pulls WRITE low, and then pulls ASTRB low to indicate that data has been sent.
3. If WAIT was high during the system write cycle, ZWS goes low and IOCHRDY stays high.
4. When the system pulls WR high, the EPP pulls ASTRB, ZWS and then WRITE to high. The EPP can change PD7-0 only when WRITE and ASTRB are high.
5. If the peripheral is fast enough to pull WAIT low before the system terminates the write cycle, the EPP pulls IOCHRDY to low, but does not pull ZWS to low, thus carrying out a normal (non-ZWS EPP 1.7) write operation.

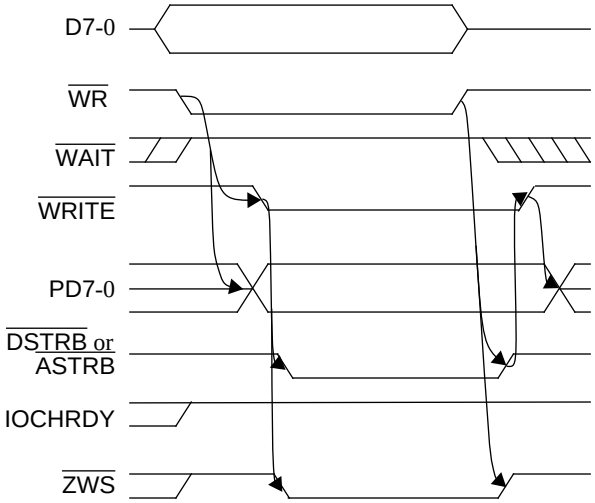


FIGURE 6-14. EPP Write with Zero Wait States

A read operation is similar, except for the data direction, activation of RD instead of WR, and WRITE stays high.

6.3.11 EPP 1.7 and 1.9 Zero Wait State Data Write and Read Operations

EPP 1.7 zero wait state data write and read operations are similar to EPP zero wait state address write and read operations, with the exception that the data strobe (DSTRB signal), and a data register, replace the address strobe (ASTRB signal) and the address register, respectively.

EPP 1.9 Address Write

The following procedure selects a peripheral or register as shown in Figure 6-15.

1. The system writes a byte to the EPP Address register.
2. The EPP pulls IOCHRDY low, and waits for WAIT to become low.
3. When WAIT becomes low, the EPP pulls WRITE to low and drives the latched byte onto PD7-0. If WAIT was already low, steps 2 and 3 occur concurrently.
4. The EPP pulls ASTRB low and waits for WAIT to become high.
5. When WAIT becomes high, the EPP stops pulling IOCHRDY low, and waits for WR to become high.
6. When WR becomes high, the EPP pulls ASTRB high, and waits for WAIT to become low.
7. If no EPP write is pending when WAIT becomes low, the EPP pulls WRITE to high. Otherwise, WRITE remains low, and the EPP may change PD7-0.

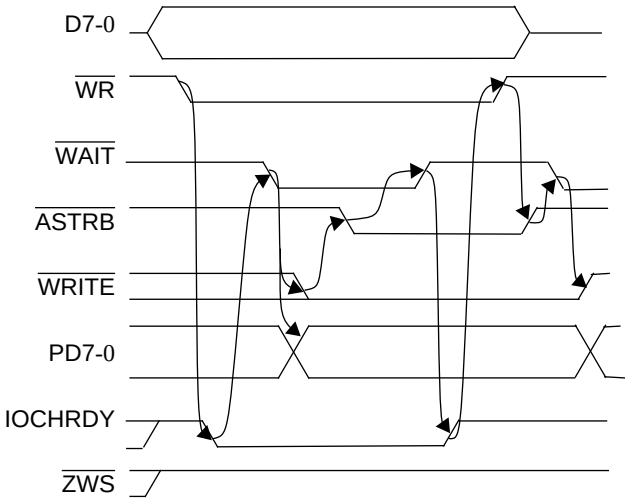


FIGURE 6-15. EPP 1.9 Address Write

EPP 1.9 Address Read

The following procedure reads from the address register.

1. The system reads a byte from the EPP address register. When RD becomes low, the EPP pulls IOCHRDY low, and waits for WAIT to become low.
2. When WAIT becomes low, the EPP pulls ASTRB low and waits for WAIT to become high. If WAIT was already low, steps 2 and 3 occur concurrently.
3. When WAIT becomes high, the EPP stops pulling IOCHRDY low, and waits for RD to become high.
4. When RD becomes high, the EPP latches PD7-0 (to provide sufficient hold time), pulls ASTRB high, and puts D7-0 in TRI-STATE.

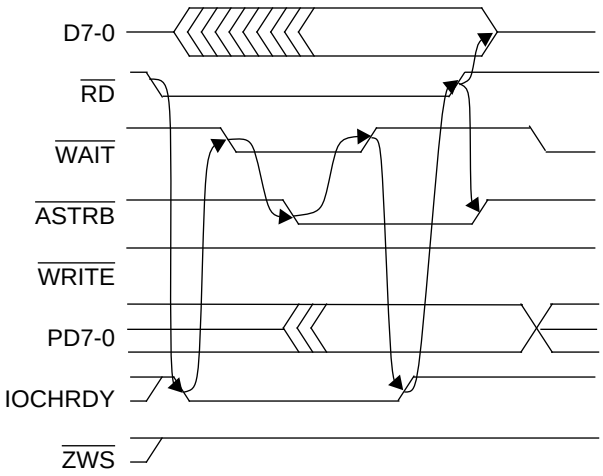


FIGURE 6-16. EPP 1.9 Address Read

EPP 1.9 Data Write and (Backward) Data Read

This procedure writes to the selected peripheral drive or register.

EPP 1.9 data read and write operations are similar to EPP 1.9 address read and write operations, except that the data strobe (DSTRB signal) and EPP Data register replace the address strobe (ASTRB signal) and the EPP Address register, respectively.

6.4 EXTENDED CAPABILITIES PARALLEL PORT (ECP)

In the Extended Capabilities Port (ECP) modes, the device is a state machine that supports a 16-byte FIFO that can be configured for either direction, command and data FIFO tags (one per byte), a FIFO threshold interrupt for both directions, FIFO empty and full status bits, automatic generation of strobes (by hardware) to fill or empty the FIFO, transfer of commands and data, and Run Length Encoding (RLE) expanding (decompression) as explained below. The FIFO can be accessed by PIO or system DMA cycles.

6.4.1 ECP Modes

ECP modes are enabled at as described in Table 6-1 on page 85. The ECP mode is selected at reset by setting bits 7-5 of the SuperI/O Parallel Port Configuration register at index F0h (see Section 2.7.1 on page 24) to 100 or 111. Thereafter, the mode is controlled via the bits 7-5 of the ECP Extended Control Register (ECR) at offset 402h of the parallel port. See Section 6.5.12 on page 97.

Table 6-9 lists the ECP modes. See Table 6-11 on page 102 and Section 6.6 on page 101 for more detailed descriptions of these modes.

6.4.2 Software Operation

Software should operate as described in "*Extended Capabilities Port Protocol and ISA Interface Standard*".

Some of these operations are:

- Software should enable ECP after bits 3-0 of the parallel port Control Register (CTR) are set to 0100.
- When ECP is enabled, software should switch modes only through modes 000 or 001.
- When ECP is enabled, the software should change direction only in mode 001.
- Software should not switch from mode 010 or 011, to mode 000 or 001, unless the FIFO is empty.
- Software should switch to mode 011 when bits 0 and 1 of DCR are 0.
- Software should switch to mode 010 when bit 0 of DCR is 0.
- Software should disable ECP only in mode 000 or 001.

5. Software should switch to mode 100 when bits 0, 1 and 3 of the DCR are 0.
6. Software should switch from mode 100 to mode 000 or 001 only when bit 7 of the DSR (BUSY) is 1. Otherwise, an on-going EPP cycle can be aborted.
7. When the ECP is in mode 100, software should write 0 to bit 5 of the DCR before performing EPP cycles.

Software may switch from mode 011 backward to modes 000 or 001, when there is an on-going ECP read cycle. In this case, the read cycle is aborted by deasserting AFD. The FIFO is reset (empty) and a potential byte expansion (RLE) is automatically terminated since the new mode is 000 or 001.

6.4.3 Hardware Operation

The ZWS signal is asserted by the ECP when ECP modes are enabled, and an ECP register is accessed by system PIO instructions, thus using a system zero wait states cycle (except during read cycles from ECR).

The ECP uses an internal clock, which can be frozen to reduce power consumption during power down. In this power-down state the DMA is disabled, all interrupts (except ACK) are masked, and the FIFO registers are not accessible (access is ignored). The other ECP registers are unaffected by power-down and are always accessible when the ECP is enabled. During power-down the FIFO status and contents become inaccessible, and the system reads bit 2 of ECR as 0, bit 1 of ECR as 1 and bit 0 of ECR as 1, regardless of the actual values of these bits. The FIFO status and contents are not lost, however, and when the clock activity resumes, the values of these bits resume their designated functions.

When the clock is frozen, an on-going ECP cycle may be corrupted, but the next ECP cycle will not start even if the FIFO is not empty in the forward direction, or not full in the backward direction. If the ECP clock starts or stops toggling during a system cycle that accesses the FIFO, the cycle may yield wrong data.

ECP output signals are inactive when the ECP is disabled.

Only the FIFO, DMA and RLE do not function when the clock is frozen. All other registers are accessible and functional. The FIFO, DMA and RLE are affected by ECR modifications, i.e., they are reset when exits from modes 010 or 011 are carried out even while the clock is frozen.

6.5 ECP MODE REGISTERS

The ECP registers are each a byte wide, and are listed in Table 6-6 in order of their offsets from the base address of the parallel port. In addition, the ECP has control registers at second level offsets, that are accessed via the EIR and EDR registers. See Section 6.5.2 on page 93.

TABLE 6-6. Extended Capabilities Parallel Port (ECP) Registers

Offset	Symbol	Description	Modes (ECR Bits) 7 6 5	R/W
000h	DATAR	Parallel Port Data Register	0 0 0 0 0 1	R/W
000h	AFIFO	ECP Address FIFO	0 1 1	W
001h	DSR	Status Register	All Modes	R
002h	DCR	Control Register	All Modes	R/W
400h	CFIFO	Parallel Port Data FIFO	0 1 0	W
400h	DFIFO	ECP Data FIFO	0 1 1	R/W
400h	TFIFO	Test FIFO	1 1 0	R/W
400h	CNFGA	Configuration Register A	1 1 1	R
401h	CNFGB	Configuration Register B	1 1 1	R
402h	ECR	Extended Control Register	All Modes	R/W
403h	EIR	Extended Index Register	All Modes	R/W
404h	EDR	Extended Data Register	All Modes	R/W
405h	EAR	Extended Auxiliary Status Register	All Modes	R/W
Control Registers at Second Level Offsets				
00h	Control0		All Modes	R/W
02h	Control2		All Modes	R/W
04h	Control4		All Modes	R/W
05h	PP Confg0		All Modes	R/W

6.5.1 Accessing the ECP Registers

The AFIFO, CFIFO, DFIFO and TFIFO registers access the same ECP FIFO. The FIFO is accessed at Base + 000h, or Base + 400h, depending on the mode field of ECR and the register.

The FIFO can be accessed by system DMA cycles, as well as system PIO cycles.

When the DMA is configured and enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0) the ECP automatically (by hardware) issues DMA requests to fill the FIFO (in the forward direction when bit 5 of DCR is 0) or to empty the FIFO (in the backward direction when bit 5 of DCR is 1). All DMA transfers are to or from these registers. The ECP does not assert DMA requests for more than 32 consecutive DMA cycles. The ECP stops requesting the DMA when TC is detected during an ECP DMA cycle.

A “Demand DMA” feature reduces system overhead caused by DMA data transfers. When this feature is enabled by bit 6 of the PP Config0 register at second level offset 05h, it prevents servicing of DMA requests until after four have accumulated and are held pending. See “Bit 6 - Demand DMA Enable” on page 101.

Writing into a full FIFO, and reading from an empty FIFO, are ignored. The written data is lost, and the read data is undefined. The FIFO empty and full status bits are not affected by such accesses.

Some registers are not accessible in all modes of operation, or may be accessed in one direction only. Accessing a non accessible register has no effect. Data read is undefined; data written is ignored; and the FIFO does not update. The SPP registers (DTR, STR and CTR) are not accessible when the ECP is enabled.

To improve noise immunity in ECP cycles, the state machine does not examine the control handshake response lines until the data has had time to switch.

In ECP modes:

- DATAR replaces DTR of SPP/EPP
- DSR replaces STR of SPP/EPP
- DCR replaces CTR of SPP/EPP

6.5.2 Second Level Offsets

The EIR, EDR, and EAR registers support enhanced control and status features. When bit 4 of the Parallel Port Configuration register is 1 (as described in Section 2.7.1 on page 24), EIR and EDR serve as index and data registers, respectively.

EIR and EDR at offsets 403 and 404, respectively, access the control registers (Control0, Control2, Control4 and PP Config0) at second level offsets 00h, 02h, 04h and 05h, respectively. These control registers are functional only. Accessing these registers is possible when bit 4 of the SuperI/O Parallel Port Configuration register at index F0h of logical device 4 is1 and when bit 2 or 10 of the base address is 1.

6.5.3 ECP Data Register (DATAR), Bits 7-5 of ECR = 000 or 001, Offset 000h

The ECP Data Register (DATAR) register is the same as the DTR register (see Section 6.2.2), except that a read always returns the values of the PD7-0 signals instead of the register latched data.

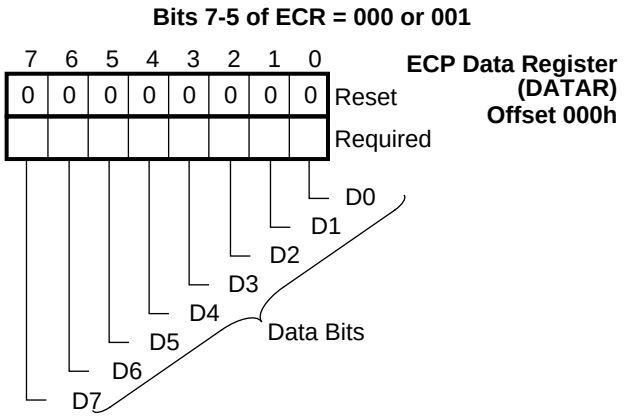


FIGURE 6-17. DATAR Register Bitmap

6.5.4 ECP Address FIFO (AFIFO) Register, Bits 7-5 of ECR = 011, Offset 000h

The ECP Address FIFO Register (AFIFO) is write only. In the forward direction (when bit 5 of DCR is 0) a byte written into this register is pushed into the FIFO and tagged as a command.

Reading this register returns undefined contents. Writing to this register in a backward direction (when bit 5 of DCR is 1) has no effect and the data is ignored.

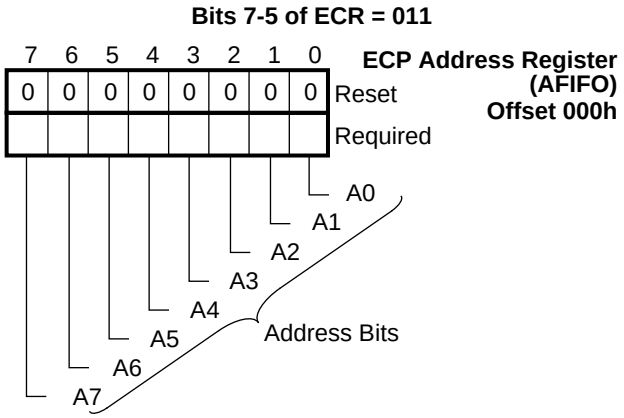


FIGURE 6-18. AFIFO Register Bitmap

6.5.5 ECP Status Register (DSR), Offset 001h

This read-only register displays device status. Writes to this DSR have no effect and the data is ignored.

This register should not be confused with the DSR register of the Floppy Disk Controller (FDC).

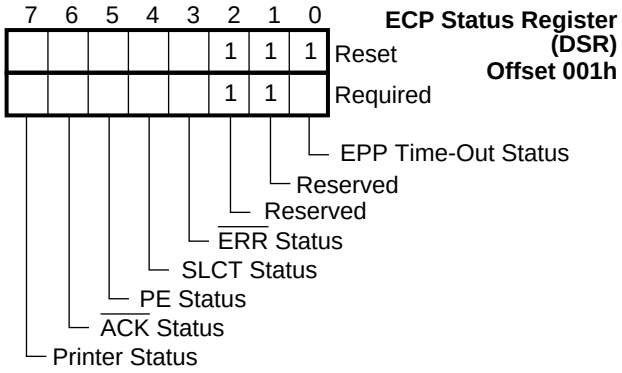


FIGURE 6-19. ECP DSR Register Bitmap

Bits 0 - EPP Time-Out Status

In EPP modes only, this is the time-out status bit. In all other modes this bit has no function and has the constant value 1.

This bit is cleared when an EPP mode is enabled. Thereafter, this bit is set to 1 when a time-out occurs in an EPP cycle and is cleared when STR is read.

In EPP modes:

0 - An EPP mode is set. No time-out occurred since STR was last read.

1 - Time-out occurred on EPP cycle (minimum of 10 µsec). (Default)

Bits 2,1 - Reserved

These bits are reserved and are always 1.

Bit 3 - $\overline{\text{ERR}}$ Status

This bit reflects the status of the $\overline{\text{ERR}}$ signal.

0 - Printer error.

1 - No printer error.

Bit 4 - SLCT Status

This bit reflects the status of the Select signal. The printer sets this signal high when it is online and selected

0 - Printer not selected. (Default)

1 - Printer selected and on-line.

Bit 5 - PE Status

This bit reflects the status of the Paper End (PE) signal.

0 - Paper not ended.

1 - No paper in printer.

Bit 6 - $\overline{\text{ACK}}$ Status

This bit reflects the status of the $\overline{\text{ACK}}$ signal. This signal is pulsed low after a character is received.

0 - Character received.

1 - No character received. (Default)

Bit 7 -Printer Status

This bit reflects the inverse of the state of the BUSY signal.

0 - Printer is busy (cannot accept another character now).

1 - Printer not busy (ready for another character).

6.5.6 ECP Control Register (DCR), Offset 002h

Reading this register returns the register content (not the signal values, as in SPP mode).

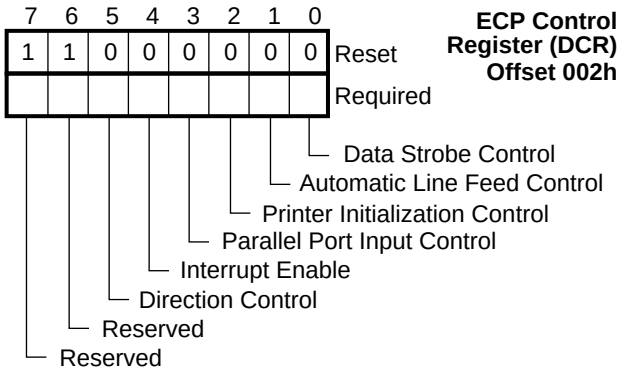


FIGURE 6-20. DCR Register Bitmap

Bit 0 - Data Strobe Control

Bit 0 directly controls the data strobe signal to the printer via the $\overline{STB}$ signal. It is the inverse of the $\overline{STB}$ signal.

0 - The $\overline{STB}$ signal is inactive in all modes except 010 and 011. In these modes, it may be active or inactive as set by the software.

1 - In all modes, $\overline{STB}$ is active.

Bit 1 - Automatic Line Feed Control

This bit directly controls the automatic feed XT signal to the printer via the $\overline{AFD}$ signal. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the $\overline{AFD}$ signal.

In mode 011, $\overline{AFD}$ is activated by both ECP hardware and by software using this bit.

0 - No automatic line feed. (Default)

1 - Automatic line feed.

Bit 2 - Printer Initialization Control

Bit 2 directly controls the signal to initialize the printer via the $\overline{INIT}$ signal. Setting this bit to low initializes the printer. The $\overline{INIT}$ signal follows this bit.

0 - Initialize printer. (Default)

1 - Printer initialized.

Bit 3 - Parallel Port Input Control

This bit directly controls the select input device signal to the printer via the $\overline{SLIN}$ signal. It is the inverse of the $\overline{SLIN}$ signal.

This bit must be set to 1 before enabling the EPP or ECP modes.

0 - The printer is not selected.

1 - The printer is selected.

Bit 4 - Interrupt Enable

Bit 4 enables the interrupt generated by the $\overline{ACK}$ signal. In ECP mode, this bit should be set to 0. This bit does not float the IRQ pin.

0 - Masked. (Default)

1 - Enabled.

Bit 5 - Direction Control

This bit determines the direction of the parallel port.

This is a read/write bit in EPP mode. In SPP mode it is a write only bit. A read from it returns 1. In SPP Compatible mode and in EPP mode it does not control the direction. See Table 6-4.

The ECP drives the PD7-0 pins in the forward direction, but does not drive them in the backward direction.

This bit is readable and writable. In modes 000 and 010 the direction bit is forced to 0, internally, regardless of the data written into this bit.

0 - ECP drives forward in output mode. (Default)

1 - ECP direction is backward.

Bits 7,6 - Reserved

These bits are reserved and are always 1.

6.5.7 Parallel Port Data FIFO (CFIFO) Register, Bits 7-5 of ECR = 010, Offset 400h

The Parallel Port FIFO (CFIFO) register is write only. A byte written to this register by PIO or DMA is pushed into the FIFO and tagged as data.

Reading this register has no effect and the data read is undefined.

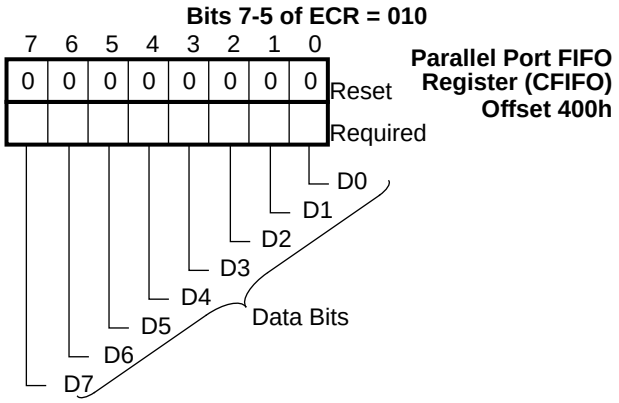


FIGURE 6-21. CFIFO Register Bitmap

6.5.8 ECP Data FIFO (DFIFO) Register, Bits 7-5 of ECR = 011, Offset 400h

This bi-directional FIFO functions as either a write-only device when bit 5 of DCR is 0, or a read-only device when it is 1.

In the forward direction (bit 5 of DCR is 0), a byte written to the ECP Data FIFO (DFIFO) register by PIO or DMA is pushed into the FIFO and tagged as data. Reading this register when set for write-only has no effect and the data read is undefined.

In the backward direction (bit 5 of DCR is 1), the ECP automatically issues ECP read cycles to fill the FIFO.

Reading from this register pops a byte from the FIFO. Writing to this register when it is set for read-only has no effect, and the data written is ignored.

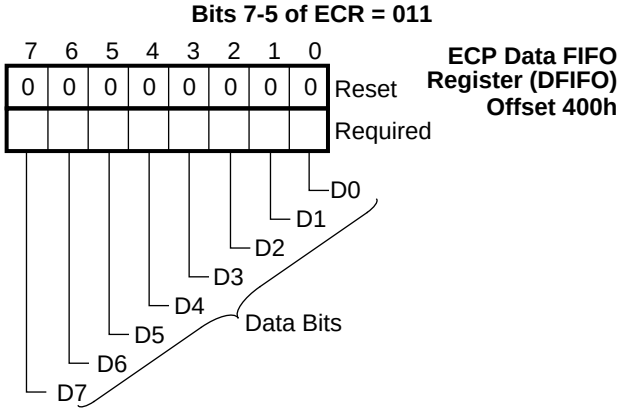


FIGURE 6-22. DFIFO Register Bitmap

6.5.9 Test FIFO (TFIFO) Register, Bits 7-5 of ECR = 110, Offset 400h

A byte written into the Test FIFO (TFIFO) register is pushed into the FIFO. A byte read from this register is popped from the FIFO. The ECP does not issue an ECP cycle to transfer the data to or from the peripheral device.

The TFIFO is readable and writable in both directions. In the forward direction (bit 5 of DCR is 0) PD7-0 are driven, but the data is undefined.

The FIFO does not stall when overwritten or underrun (access is ignored). Bytes are always read from the top of the FIFO, regardless of the direction bit setting (bit 5 of DCR). For example if 44h, 33h, 22h, 11h is written into the FIFO, reading the FIFO returns 44h, 33h, 22h, 11h (in the same order it was written).

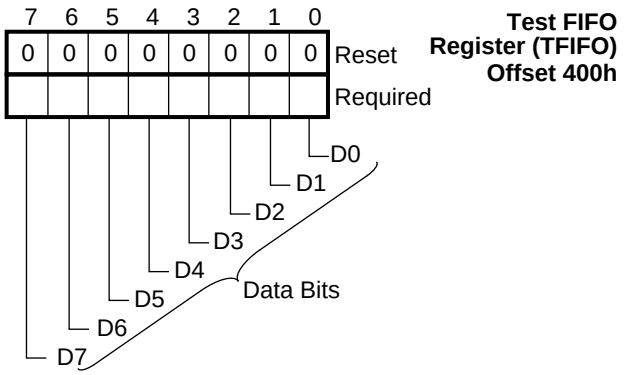


FIGURE 6-23. TFIFO Register Bitmap

6.5.10 Configuration Register A (CNFGA), Bits 7-5 of ECR = 111, Offset 400h

This register is read only. Reading CNFGA always returns 100 on bits 2 through 0 and 0001 on bits 7 through 4.

Writing this register has no effect and the data is ignored.

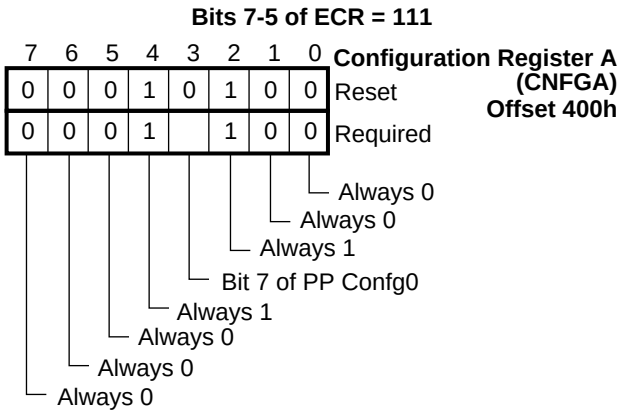


FIGURE 6-24. CNFGA Register Bitmap

Bits 2-0 - Reserved

These bits are reserved and are always 100.

Bit 3 - Bit 7 of PP Confg0

This bit reflects the value of bit 7 of the ECP PP Confg0 register (second level offset 05h), which has no specific function. Whatever value is put in bit 7 of PP Confg0 will appear in this bit.

This bit reflects a specific system configuration parameter, as opposed to other devices, e.g., 8-bit data word length.

Bit 7-4 - Reserved

These bits are reserved and are always 0001.

6.5.11 Configuration Register B (CNFGB), Bits 7-5 of ECR = 111, Offset 401h

Configuration register B (CNFGB) is read only. Reading this register returns the configured parallel port interrupt line and DMA channel, and the state of the interrupt line.

Writing to this register has no effect and the data is ignored.

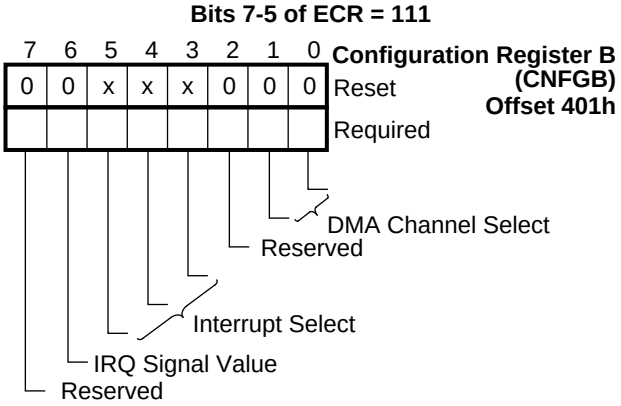


FIGURE 6-25. CNFGB Register Bitmap

Bits 1,0 - DMA Channel Select

These bits reflect the value of bits 1,0 of the PP Config0 register (second level offset 05h). Microsoft's ECP Protocol and ISA Interface Standard defines these bits as shown in Table 6-7.

Bits 1,0 of PP Config0 are read/write bits, but CNFGB bits are read only.

Upon reset, these bits are initialized to 00.

TABLE 6-7. ECP Mode DMA Selection

Bit 1	Bit 0	DMA Configuration
0	0	8-bit DMA selected by jumpers. (Default)
0	1	DMA channel 1 selected.
1	0	DMA channel 2 selected.
1	1	DMA channel 3 selected.

Bit 2 - Reserved

This bit is reserved and is always 0.

Bits 5-3 - Interrupt Select Bits

These bits reflect the value of bits 5-3 of the PP Config0 register at second level index 05h. Microsoft's ECP Protocol and ISA Interface Standard defines these bits as shown in Table 6-8.

Bits 5-3 of PP Config0 are read/write bits, but CNFGB bits are read only.

Upon reset, these bits have undefined values.

TABLE 6-8. ECP Mode Interrupt Selection

Bit 5	Bit 4	Bit 3	Interrupt Selection
0	0	0	Selected by jumpers.
0	0	1	IRQ7 selected.
0	1	0	IRQ9 selected.
0	1	1	IRQ10 selected.
1	0	0	IRQ11 selected.
1	0	1	IRQ14 selected.
1	1	0	IRQ15 selected.
1	1	1	IRQ5 selected.

Bit 6 - IRQ Signal Value

This bit holds the value of the IRQ signal configured by the Interrupt Select register (index 70h of this logical device).

Bit 7 - Reserved

This bit is reserved and is always 0.

6.5.12 Extended Control Register (ECR), Offset 402h

This register controls the ECP and parallel port functions. On reset this register is initialized to 00010101. IOCHRDY is driven low on an ECR read when the ECR status bits do not hold updated data.

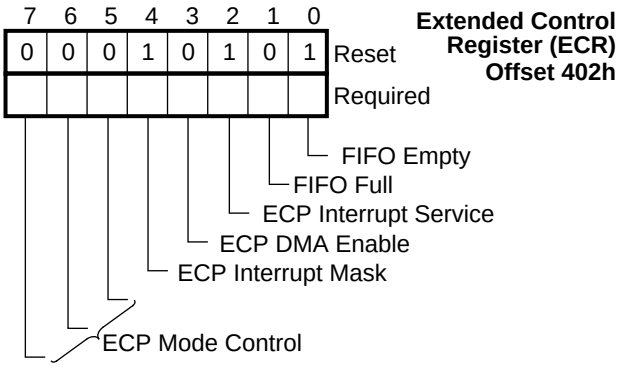


FIGURE 6-26. ECR Register Bitmap

Bit 0 - FIFO Empty

This bit continuously reflects the FIFO state, and therefore can only be read. Data written to this bit is ignored.

When the ECP clock is frozen this bit is read as 1, regardless of the actual FIFO state.

0 - The FIFO has at least one byte of data.

1 - The FIFO is empty or ECP clock is frozen.

Bit 1 - FIFO Full

This bit continuously reflects the FIFO state, and therefore can only be read. Data written to this bit is ignored.

When the ECP clock is frozen this bit is read as 1, regardless of the actual FIFO state.

0 - The FIFO has at least one free byte.

1 - The FIFO is full or ECP clock frozen.

Bit 2 - ECP Interrupt Service

This bit enables servicing of interrupt requests. It is set to 1 upon reset, and by the occurrence of interrupt events. It is set to 0 by software.

While this bit is 1, neither the DMA nor the interrupt events listed below will generate an interrupt.

While this bit is 0, the interrupt setup is "armed" and an interrupt is generated on occurrence of an interrupt event.

While the ECP clock is frozen, this bit always returns a 0 value, although it retains its proper value and may be modified.

When one of the following interrupt events occurs while this bit is 0, an interrupt is generated and this bit is set to 1 by hardware.

— DMA is enabled (bit 3 of ECR is 1) and terminal count is reached.

— FIFO write threshold reached (no DMA - bit 3 of ECR is 0; forward direction (bit 5 of DCR is 0), and there are eight or more bytes free in the FIFO).

— FIFO read threshold reached (no DMA - bit 3 of ECR is 0; read direction set - bit 5 of DCR is 1, and there are eight or more bytes to read from the FIFO).

0 - The DMA and the above interrupts are not disabled.

1 - The DMA and the above three interrupts are disabled.

Bit 3 - ECP DMA Enable

0 - The DMA request signal (DRQ3-0) is set to TRI-STATE and the appropriate acknowledge signal (DACK3-0) is assumed inactive.

1 - The DMA is enabled and the DMA starts when bit 2 of ECR is 0.

Bit 4 - ECP Interrupt Mask

0 - An interrupt is generated on $\overline{ERR}$ assertion (the high-to-low edge of $\overline{ERR}$). An interrupt is also generated while $\overline{ERR}$ is asserted when this bit is changed from 1 to 0; this prevents the loss of an interrupt between ECR read and ECR write.

1 - No interrupt is generated.

Bits 7-5 - ECP Mode Control

These bits set the mode for the ECP device. See Section 6.6 for a more detailed description of operation in each of these ECP modes. The ECP modes are listed in Table 6-9 and described in detail in Table 6-11.

TABLE 6-9. ECP Modes Encoding

ECR Bit Encoding			Mode Name
Bit 7	Bit 6	Bit 5	
0	0	0	Standard
0	0	1	PS/2
0	1	0	Parallel Port FIFO
0	1	1	ECP FIFO
1	0	0	EPP Mode
1	1	0	FIFO Test
1	1	1	Configuration

6.5.13 ECP Extended Index Register (EIR), Offset 403h

The parallel port is partially configured by bits within the logical device address space. These configuration bits are accessed via this read/write register and the Extended Data Register (EDR) (see Section 6.5.14), when bit 4 of the SuperI/O Parallel Port Configuration register at index F0h of logical device 4 is set to 1. See Section 2.7.1 on page 24.

The configuration bits within the parallel port address space are initialized to their default values on reset, and not when the parallel port is activated.

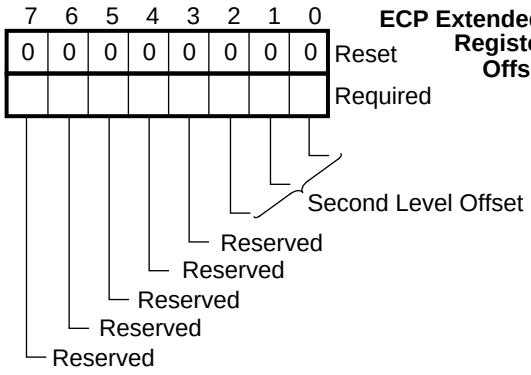


FIGURE 6-27. EIR Register Bitmap

Bits 2-0 - Second Level Offset

Data written to these bits is used as a second level offset for accesses to a specific control register. Second level offsets of 00h, 02h, 04h and 05h are supported. Attempts to access registers at any other offset have no effect.

TABLE 6-10. Second Level Offsets

Second Level Offset	Control Register Name	Described in Section
00h	Control0	6.5.16 on page 99
02h	Control2	6.5.17 on page 99
04h	Control4	6.5.18 on page 100
05h	PP Confg0	6.5.19 on page 100

000 - Access the Control0 register.

010 - Access the Control2 register.

100 - Access the Control4 register.

101 - Access the PP Confg0 register.

Bits 7-3 - Reserved

These bits are treated as 0 for offset calculations. Writing any other value to them has no effect.

These bits are read only. They return 00000 on reads and must be written as 00000.

6.5.14 ECP Extended Data Register (EDR), Offset 404h

This read/write register is the data port of the control register indicated by the index stored in the EIR. Reading or writing this register reads or writes the data in the control register whose second level offset is specified by the EIR.

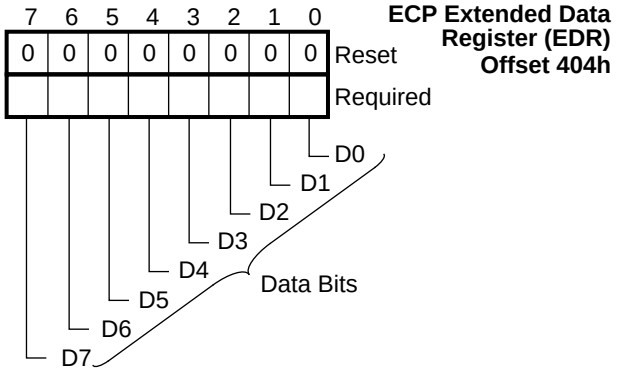


FIGURE 6-28. EDR Register Bitmap

Bits 7-0 - Data Bits

These read/write data bits transfer data to and from the Control Register pointed at by the EIR register.

6.5.15 ECP Extended Auxiliary Status Register (EAR), Offset 405h

Upon reset, this register is initialized to 00h.

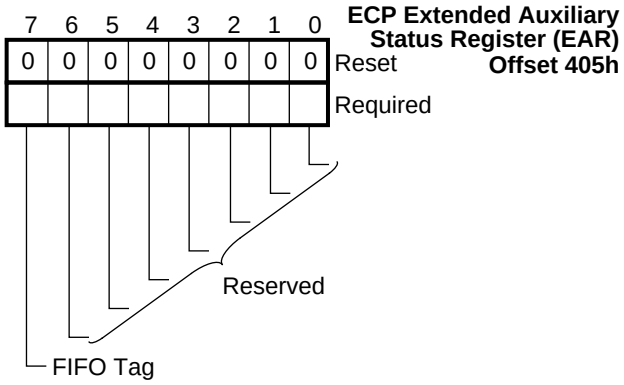


FIGURE 6-29. EAR Register Bitmap

Bits 6-0 - Reserved

These bits are reserved.

Bit 7 - FIFO Tag

Read only. In mode 011, when bit 5 of the DCR is 1 (backward direction), this bit reflects the value of the tag bit (BUSY status) of the word currently in the bottom of the FIFO.

In other modes this bit is indeterminate.

6.5.16 Control0, Second Level Offset 00h

Upon reset, this register is initialized to 00h.

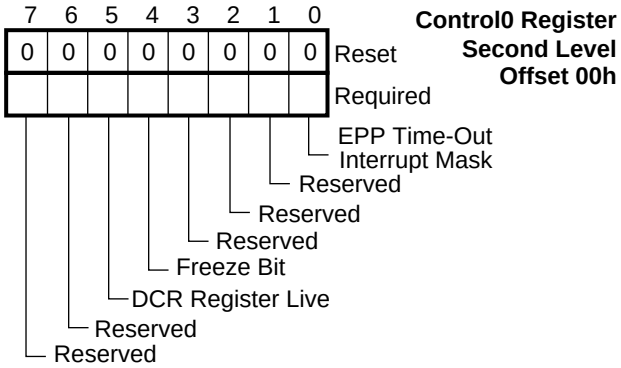


FIGURE 6-30. Control0 Register Bitmap

Bit 0 - EPP Time-Out Interrupt Mask

0 - The EPP time-out is masked.

1 - The EPP time-out is generated.

Bit 3-1 - Reserved

This bit is reserved.

Bit 4 - Freeze Bit

In mode 011, setting this bit to 1 freezes part of the interface with the peripheral device, and clearing this bit to 0 releases and initializes it.

In all other modes the value of this bit is ignored.

Bit 5 - DCR Register Live

When this bit is 1, reading the DCR (see 6.5.6 on page 95) reads the interface control lines pin values regardless of the mode selected.

Otherwise, reading the DCR reads the content of the register.

Bits 7, 6 - Reserved

This bit is reserved.

6.5.17 Control2, Second Level Offset 02h

Upon reset, this register is initialized to 00h.

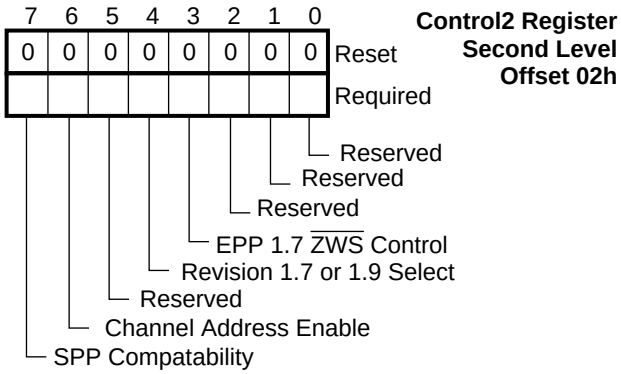


FIGURE 6-31. Control2 Register Bitmap

Bits 2-0 - Reserved

These bits are reserved.

Bit 3 - EPP 1.7 $\overline{\text{ZWS}}$ Control

Upon reset this bit is initialized to 0. This bit controls assertion of $\overline{\text{ZWS}}$ on EPP 1.7 access.

There is no $\overline{\text{ZWS}}$ assertion on SPP and on EPP 1.9 access. $\overline{\text{ZWS}}$ is always asserted on ECP access.

Control of $\overline{\text{ZWS}}$ assertion on parallel port access, except in EPP mode, is done via the SuperI/O Configuration 1 register. See 2.4.1 on page 21.

0 - $\overline{\text{ZWS}}$ not asserted on EPP 1.7 access.

1 - $\overline{\text{ZWS}}$ asserted on EPP 1.7 access.

Bit 4 - EPP 1.7/1.9 Select

Selects EPP version 1.7 or 1.9.

0 - EPP version 1.7.

1 - EPP version 1.9.

Bit 5 - Reserved

This bit is reserved.

Bit 6 - Channel Address Enable

When this bit is 1, mode is 011, direction is backward, there is an input command (BUSY is 0), and bit 7 of the data is 1, the command is written into the FIFO.

Bit 7 - SPP Compatibility

See the Mode Select field (bits 7 through 5 of the ECR register) on page 98 for a description of each mode.

0 - Modes 000, 001 and 100 are identical to SPP.

1 - Modes 000 and 001 of the ECP are identical with Compatible and Extended modes of the SPP (see Section 6.1 on page 84), and mode 100 of the ECP is compatible with EPP mode.

Modes 000, 001 and 100 differ as follows:

000, 001 and 100 – Reading DCR returns pin values of bits 3-0.

000 and 001 – Reading DCR returns 1 for bit 5.

000, or 001 or 100 when bit 5 of DCR is 0 (forward direction) – Reading DATAR returns register latched value instead of pin values.

000, 001, and 100, when bit 4 of DCR is 0 – IRQx is floated.

001 – $\overline{\text{IRQx}}$ is a level interrupt generated on the trailing edge of $\overline{\text{ACK}}$. Bit 2 of the DSR is the IRQ status bit (same behavior as bit 2 of the STR).

6.5.18 Control4, Second Level Offset 04h

Upon reset this register is initialized to 00000111.

This register enables control of the fairness mechanism of the DMA by programming the maximum number of bus cycles that the parallel port DMA request signals can remain active, and the minimum number of clock cycles that they will remain inactive after they were deactivated.

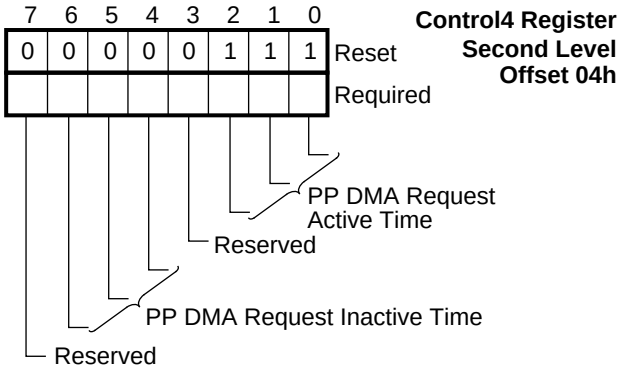


FIGURE 6-32. Control4 Register Bitmap

Bits 2- 0 - Parallel Port DMA Request Active Time

This field specifies the maximum number of consecutive bus cycles that the parallel port DMA signals can remain active.

The default value is 111, which specifies 32 cycles.

When these bits are 0, the number is 1 cycle.

Otherwise, the number is 4(n+1) where n is the value of these bits.

Bit 3 - Reserved

This bit is reserved.

Bits 6-4 - Parallel Port DMA Request Inactive Time

This field specifies the minimum number of clock cycles that the parallel port DMA signals remain inactive after being deactivated by the fairness mechanism.

The default value is 000, which specifies 8 clock cycles.

Otherwise, the number of clock cycles is 8 + 32n, where n is the value of these bits.

Bit 7 - Reserved

This bit is reserved.

6.5.19 PP Confg0, Second Level Offset 05h

Upon reset this register is initialized to 00h.

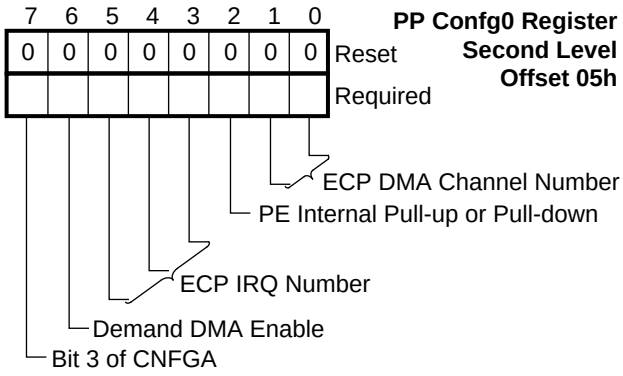


FIGURE 6-33. PP Confg0 Register Bitmap

Bits 1, 0 - ECP DMA Channel Number

These bits identify the ECP DMA channel number, as reflected on bits 1 and 0 of the ECP CNFGB register. See Section 6.5.11 on page 96. Actual ECP DMA routing is controlled by the DMA channel select register (index 74h) of this logical device.

Microsoft's ECP protocol and ISA interface standard define bits 1 and 0 of CNFGB as shown in Table 6-7 on page 97.

Bit 2 - Paper End (PE) Internal Pull-up or Pull-down Resistor Select

0 - PE has a nominal 25 KΩ internal pull-down resistor.

1 - PE has a nominal 25 KΩ internal pull-up resistor.

Bits 5- 3 - ECP IRQ Number

These bits identify the ECP IRQ number, as reflected on bits 5 through 3 of the ECP CNFGB register. See Section 6.5.11 on page 96. Actual ECP IRQ routing is controlled by interrupt select register (index 70h) of this logical device.

Microsoft's ECP protocol and ISA interface standard defines bits 5 through 3 of CNFGB, as shown in 6-8 on page 97.

Bit 6 - Demand DMA Enable

If enabled, DRQ is asserted when a FIFO threshold of 4 is reached or when flush-time-out expires, except when DMA fairness prevents DRQ assertion. The threshold of 4 is for four empty entries forward and for four valid entries backward.

Once DRQ is asserted, it is held asserted for four DMA transfers, as long as the FIFO is able to process these four transfers, i.e., FIFO not empty backward.

When these four transfers are done, the DRQ behaves as follows:

— If DMA fairness prevents DRQ assertion (as in the case of 32 consecutive DMA transfers) then DRQ becomes low.

— If the FIFO is not able to process another four transfers (below threshold), then DRQ is becomes low.

— If the FIFO is able to process another four transfers (still above the threshold and no fairness to prevent DRQ assertion), then DRQ is held asserted as detailed above.

The flush time-out is an 8-bit counter that counts 256 clocks of 24 MHz and triggers DRQ assertion when the terminal-count is reached, i.e., when flush time-out expires). The counter is enabled for counting backward when the peripheral state machine writes a byte and DRQ is not asserted. Once enabled, it counts the 24 MHz clocks. The counter is reset and disabled when DRQ is asserted. The counter is also reset and disabled for counting forward and when demand the DMA is disabled.

This mechanism is reset whenever ECP mode is changed, the same way the FIFO is flushed in this case.

0 - Disabled.

1 - Enabled.

Bit 7 - Bit 3 of CNFGA

This bit may be utilized by the user. The value of this bit is reflected on bit 3 of the ECP CNFGA register.

6.6 DETAILED ECP MODE DESCRIPTIONS

Table 6-11 summarizes the functionality of the ECP in each mode. The following Sections describe how the ECP functions in each mode, in detail.

6.6.1 Software Controlled Data Transfer (Modes 000 and 001)

Software controlled data transfer is supported in modes 000 and 001. The software generates peripheral-device cycles by modifying the DATAR and DCR registers and reading the DSR, DCR and DATAR registers. The negotiation phase and nibble mode transfer, as defined in the IEEE 1284 standard, are performed in these modes.

In these modes the FIFO is reset (empty) and is not functional, the DMA and RLE are idle.

Mode 000 is for the forward direction only; the direction bit (bit 5 of DCR) is forced to 0 and PD7-0 are driven. Mode 001 is for both the forward and backward directions. The direction bit controls whether or not pins PD7-0 are driven.

6.6.2 Automatic Data Transfer (Modes 010 and 011)

Automatic data transfer (ECP cycles generated by hardware) is supported only in modes 010 and 011 (Parallel Port and ECP FIFO modes). Automatic DMA access to fill or empty the FIFO is supported in modes 010, 011 and 110. Mode 010 is for the forward direction only; the direction bit is forced to 0 and PD7-0 are driven. Mode 011 is for both the forward and backward directions. The direction bit controls whether PD7-0 are driven.

Automatic Run Length Expanding (RLE) is supported in the backward direction.

Forward Direction (Bit 5 of DCR = 0)

When the ECP is in forward direction and the FIFO is not full (bit 1 of ECR is 0) the FIFO can be filled by software writes to the FIFO registers (AFIFO and DFIFO in mode 011, and CFIFO in mode 010).

When DMA is enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0) the ECP automatically issues DMA requests to fill the FIFO with data bytes (not including command bytes).

When the ECP is in forward direction and the FIFO is not empty (bit 0 of ECR is 0) the ECP pops a byte from the FIFO and issues a write signal to the peripheral device. The ECP drives $\overline{AFD}$ according to the operation mode (bits 7-5 of ECR) and according to the tag of the popped byte as follows:

- In Parallel Port FIFO mode (mode 010) $\overline{AFD}$ is controlled by bit 1 of DCR.
- In ECP mode (mode 011) $\overline{AFD}$ is controlled by the popped tag. $\overline{AFD}$ is driven high for normal data bytes and driven low for command bytes.

ECP (Forward) Write Cycle

An ECP write cycle starts when the ECP drives the popped tag onto $\overline{AFD}$ and the popped byte onto PD7-0. When BUSY is low the ECP asserts $\overline{STB}$. In 010 mode the ECP deactivates $\overline{STB}$ to terminate the write cycle. In 011 mode the ECP waits for BUSY to be high.

When BUSY is high, the ECP deactivates $\overline{STB}$, and changes $\overline{AFD}$ and PD7-0 only after BUSY is low.

TABLE 6-11. ECP Modes

ECP Mode (ECR Bits)			ECP Mode Name	Operation Description
7	6	5		
0	0	0	Standard	Write cycles are under software control. $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$ and $\overline{SLIN}$ are open-drain output signals. Bit 5 of DCR is forced to 0 (forward direction) and PD7-0 are driven. The FIFO is reset (empty). Reading DATAR returns the last value written to DATAR.
0	0	1	PS/2	Read and write cycles are under software control. The FIFO is reset (empty). $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$ and $\overline{SLIN}$ are push-pull output signals.
0	1	0	Parallel Port FIFO	Write cycles are automatic, i.e., under hardware control ($\overline{STB}$ is controlled by hardware). Bit 5 of DCR is forced to 0 internally (forward direction) and PD7-0 are driven. $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$ and $\overline{SLIN}$ are push-pull output signals.
0	1	1	ECP FIFO	The FIFO direction is automatic, i.e., controlled by bit 5 of DCR. Read and write cycles to the device are controlled by hardware ($\overline{STB}$ and $\overline{AFD}$ are controlled by hardware). $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$ and $\overline{SLIN}$ are push-pull output signals.
1	0	0	EPP	EPP mode is enabled by bits 7 through 5 of the SuperI/O Parallel Port Configuration register, as described in Section 2.7.1 on page 24. In this mode, registers DATAR, DSR, and DCR are used as registers at offsets 00h, 01h and 02h of the EPP instead of registers DTR, STR, and CTR. $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$, and $\overline{SLIN}$ are push-pull output buffers. When there is no access to one of the EPP registers (ADDR, DATA0, DATA1, DATA2 or DATA3), mode 100 behaves like mode 001, i.e., software can perform read and write cycles. The software should check that bit 7 of the DSR is 1 before reading or writing the DATAR register, to avoid corrupting an ongoing EPP cycle.
1	0	1	Reserved	
1	1	0	FIFO Test	The FIFO is accessible via the TFIFO register. The ECP does not issue ECP cycles to fill or empty the FIFO.
1	1	1	Configuration	CNFGA and CNFGB registers are accessible.

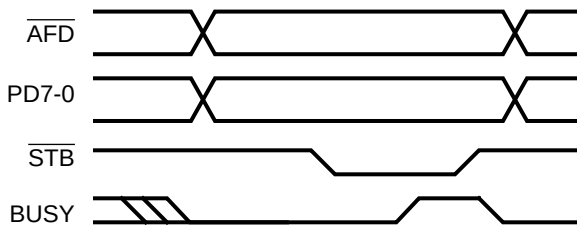


FIGURE 6-34. ECP Forward Write Cycle

Backward Direction (Bit 5 of DCR is 1)

When the ECP is in the backward direction, and the FIFO is not full (bit 1 of ECR is 0), the ECP issues a read cycle to the peripheral device and monitors the BUSY signal. If BUSY is high the byte is a data byte and it is pushed into the FIFO. If BUSY is low the byte is a command byte.

The ECP checks bit 7 of the command byte. If it is high the byte is ignored, if it is low the byte is tagged as an RLC byte (not pushed into the FIFO but used as a Run Length Count to expand the next byte read). Following an RLC read the ECP issues a read cycle from the peripheral device to read the data byte to be expanded. This byte is considered a data byte, regardless of its BUSY state (even if it is low). This byte is pushed into the FIFO (RLC+1) times (e.g. for RLC=0, push the byte once. For RLC=127 push the byte 128 times).

When the ECP is in the backward direction, and the FIFO is not empty (bit 0 of ECR is 0), the FIFO can be emptied by software reads from the FIFO register (true only for the TFIFO in mode 011, not for AFIFO or CFIFO reads).

When DMA is enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0) the ECP automatically issues DMA requests to empty the FIFO (only in mode 011).

ECP (Backward) Read Cycle

An ECP read cycle starts when the ECP drives $\overline{AFD}$ low.

The peripheral device drives BUSY high for a normal data read cycle, or drives BUSY low for a command read cycle, and drives the byte to be read onto PD7-0.

When $\overline{ACK}$ is asserted the ECP drives $\overline{AFD}$ high. When $\overline{AFD}$ is high the peripheral device deasserts $\overline{ACK}$. The ECP reads the PD7-0 byte, then drives $\overline{AFD}$ low. When $\overline{AFD}$ is low the peripheral device may change BUSY and PD7-0 states in preparation for the next cycle

.

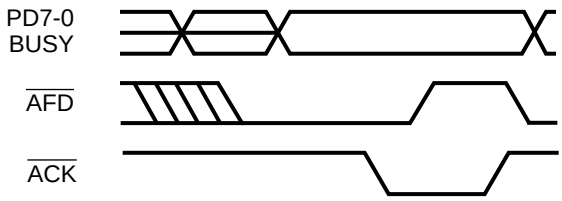


FIGURE 6-35. ECP (Backward) Read Cycle

Notes:

1. FIFO-full condition is checked before every expanded byte push.
2. Switching from modes 010 or 011 to other modes removes pending DMA requests and aborts pending RLE expansion.
3. FIFO pushes and pops are neither synchronized nor linked at the hardware level. The FIFO will not delay these operations, even if performed concurrently. Care must be taken by the programmer to utilize the empty and full FIFO status bits to avoid corrupting PD7-0 or D7-0 while a previous FIFO port access not complete.
4. In the forward direction, the empty bit is updated when the ECP cycle is completed, not when the last byte is popped from the FIFO (valid cleared on cycle end).
5. $\overline{ZWS}$ is not asserted for DMA cycles.
6. The one-bit command/data tag is used only in the forward direction.

6.6.3 Automatic Address and Data Transfers (Mode 100)

Automatic address and data transfer (EPP cycles generated by hardware) is supported in mode 100. Fast transfers are achieved by automatically generating the address and data strobes.

In this mode, the FIFO is reset (empty) and is not functional, the DMA and RLE are idle.

The direction of the automatic data transfers is determined by the $\overline{RD}$ and $\overline{WR}$ signals. The direction of software data transfer can be forward or backward, depending on bit 5 of the DCR. Bit 5 of the DCR determines the default direction of the data transfers only when there is no on-going EPP cycles.

In EPP mode 100, registers DATAR, DSR and DCR are used instead of DTR, STR and CTR respectively.

Some differences are caused by the registers. Reading DATAR returns pins values instead of register value returned when reading DTR. Reading DSR returns register value instead of pins values returned when reading STR. Writing to the DATAR during an on-going EPP 1.9 forward cycle (i.e. - when bit 7 of DSR is 1) causes the new data to appear immediately on PD7-0, instead of waiting for BUSY to become low to switch PD7-0 to the new data when writing to the DTR.

In addition, the bit 4 of the DCR functions differently relative to bit 4 of the CTR (IRQ float).

6.6.4 FIFO Test Access (Mode 110)

Mode 110 is for testing the FIFO in PIO and DMA cycles. Both read and write operations (pop and push) are supported, regardless of the direction bit.

In the forward direction PD7-0 are driven, but the data is undefined. This mode can be used to measure the system-ECP cycle throughput, usually with DMA cycles. This mode can also be used to check the FIFO depth and its interrupt threshold, usually with PIO cycles.

6.6.5 Configuration Registers Access (Mode 111)

The two configuration registers, CNFGA and CNFGB, are accessible only in this mode.

6.6.6 Interrupt Generation

An interrupt is generated when any of the events described in this section occurs. Interrupt events 2, 3 and 4 are level events. They are shaped as interrupt pulses, and are masked (inactive) when the ECP clock is frozen.

Event 1

Bit 2 of ECR is 0, bit 3 of ECR is 1 and TC is asserted during ECP DMA cycle. Interrupt event 1 is a pulse event.

Event 2

Bit 2 of ECR is 0, bit 3 of ECR is 0, bit 5 of DCR is 0 and there are eight or more bytes free in the FIFO.

This event includes the case when bit 2 of ECR is cleared to 0 and there are already eight or more bytes free in the FIFO (modes 010, 011 and 110 only).

Event 3

Bit 2 of ECR is 0, bit 3 of ECR is 0, bit 5 of DCR is 1 and there are eight or more bytes to be read from the FIFO.

This event includes the case when bit 2 of ECR is cleared to 0 and there are already eight or more bytes to be read from the FIFO (modes 011 and 110 only).

Event 4

Bit 4 of ECR is 0 and $\overline{ERR}$ is asserted (high to low edge) or $\overline{ERR}$ is asserted when bit 4 of ECR is modified from 1 to 0.

This event may be lost when the ECP clock is frozen.

Event 5

When bit 4 of DCR is 1 and $\overline{ACK}$ is deasserted (low-to-high edge).

This event behaves as in the normal SPP mode, i.e., the IRQ signal follows the $\overline{ACK}$ signal transition.

6.7 PARALLEL PORT REGISTER BITMAPS

6.7.1 EPP Modes Parallel Port Register Bitmaps

SPP or EPP Data Register (DTR) Offset 00h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

D0, D1, D2, D3, D4, D5, D6, D7 — Data Bits

EPP Data Register 0 Offset 04h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

D0, D1, D2, D3, D4, D5, D6, D7 — EPP Device Read or Write Data

SPP or EPP Status Register(STR) Offset 01h

7	6	5	4	3	2	1	0	
1	1	1	1	1	1	1	1	Reset
								Required

Time-Out Status
Reserved
IRQ Status
$\overline{\text{ERR}}$ Status
SLCT Status
PE Status
$\overline{\text{ACK}}$ Status
Printer Status

EPP Data Register 1 Offset 05h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

D8, D9, D10, D11, D12, D13, D14, D15 — EPP Device Read or Write Data

SPP or EPP Control Register (CTR) Offset 02h

7	6	5	4	3	2	1	0	
1	1	0	0	0	1	0	0	Reset
								Required

Data Strobe Control
Automatic Line Feed Control
Printer Initialization Control
Parallel Port Input Control
Interrupt Enable
Direction Control
Reserved
Reserved

EPP Data Register 2 Offset 06h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

D16, D17, D18, D19, D20, D21, D22, D23 — EPP Device Read or Write Data

EPP Address Register Offset 03h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

A0, A1, A2, A3, A4, A5, A6, A7 — EPP Device or Register Selection Address Bits

EPP Data Register 3 Offset 07h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

D24, D25, D26, D27, D28, D29, D30, D31 — EPP Device Read or Write Data

6.7.2 ECP Modes Parallel Port Register Bitmaps

Bits 7-5 of ECR = 000 or 001

ECP Data Register (DATAR) Offset 000h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

D0, D1, D2, D3, D4, D5, D6, D7 — Data Bits

Bits 7-5 of ECR = 010

Parallel Port FIFO Register (CFIFO) Offset 400h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

D0, D1, D2, D3, D4, D5, D6, D7 — Data Bits

Bits 7-5 of ECR = 011

ECP Address Register (AFIFO) Offset 000h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

A0, A1, A2, A3, A4, A5, A6, A7 — Address Bits

Bits 7-5 of ECR = 011

ECP Data FIFO Register (DFIFO) Offset 400h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

D0, D1, D2, D3, D4, D5, D6, D7 — Data Bits

ECP Status Register (DSR) Offset 001h

7	6	5	4	3	2	1	0	
					1	1	1	Reset
					1	1		Required

EPP Time-Out Status
Reserved
Reserved
$\overline{\text{ERR}}$ Status
SLCT Status
PE Status
$\overline{\text{ACK}}$ Status
Printer Status

Bits 7-5 of ECR = 110

Test FIFO Register (TFIFO) Offset 400h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

D0, D1, D2, D3, D4, D5, D6, D7 — Data Bits

ECP Control Register (DCR) Offset 002h

7	6	5	4	3	2	1	0	
1	1	0	0	0	0	0	0	Reset
								Required

Data Strobe Control
Automatic Line Feed Control
Printer Initialization Control
Parallel Port Input Control
Interrupt Enable
Direction Control
Reserved
Reserved

Bits 7-5 of ECR = 111

Configuration Register A (CNFGA) Offset 400h

7	6	5	4	3	2	1	0	
0	0	0	1	0	1	0	0	Reset
0	0	0	1		1	0	0	Required

Always 0
Always 0
Always 1
Bit 7 of PP Confg0
Always 1
Always 0
Always 0
Always 0

Bits 7-5 of ECR = 111

Configuration Register B (CNFGB) Offset 401h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- 0 — Reserved
- 0 — IRQ Signal Value
- 0, 0, 0 — Interrupt Select
- 0, 0, 0 — Reserved
- 0, 0 — DMA Channel Select

ECP Extended Auxiliary Status Register (EAR) Offset 405h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- 0 — FIFO Tag
- 0, 0, 0, 0, 0, 0, 0 — Reserved

Extended Control (ECR) Offset 402h

7	6	5	4	3	2	1	0	
0	0	0	1	0	1	0	1	Reset
								Required

- 0, 0, 0 — ECP Mode Control
- 1 — ECP Interrupt Mask
- 0 — ECP DMA Enable
- 1 — ECP Interrupt Service
- 0 — FIFO Full
- 1 — FIFO Empty

Control0 Register Second Level Offset 00h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- 0 — Reserved
- 0 — Reserved
- 0 — DCR Register Live
- 0 — Freeze Bit
- 0 — Reserved
- 0 — Reserved
- 0 — Reserved
- 0 — EPP Time-Out Interrupt Mask

ECP Extended Index Register (EIR) Offset 403h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- 0 — Reserved
- 0 — Reserved
- 0 — Reserved
- 0 — Reserved
- 0 — Reserved
- 0, 0, 0, 0 — Second Level Offset

Control2 Register Second Level Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- 0 — SPP Compatability
- 0 — Channel Address Enable
- 0 — Reserved
- 0 — Revision 1.7 or 1.9 Select
- 0 — EPP 1.7 $\overline{\text{ZWS}}$ Control
- 0 — Reserved
- 0 — Reserved
- 0 — Reserved

ECP Extended Data Register (EDR) Offset 404h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

- D7, D6, D5, D4, D3, D2, D1, D0 — Data Bits

6.8 PARALLEL PORT PIN/SIGNAL LIST

Table 6-12 shows the standard 25-pin, D-type connector definition for various parallel port operations.

TABLE 6-12. Parallel Port Pinout

Connector Pin	Pin No.	SPP, ECP Mode	I/O	EPP Mode	I/O
1	112	$\overline{STB}$	I/O	$\overline{WRITE}$	I/O
2	122	PD0	I/O	PD0	I/O
3	123	PD1	I/O	PD1	I/O
4	124	PD2	I/O	PD2	I/O
5	125	PD3	I/O	PD3	I/O
6	126	PD4	I/O	PD4	I/O
7	127	PD5	I/O	PD5	I/O
8	128	PD6	I/O	PD6	I/O
9	129	PD7	I/O	PD7	I/O
10	113	$\overline{ACK}$	I	$\overline{ACK}$	I
11	111	BUSY	I	$\overline{WAIT}$	I
12	115	PE	I	PE	I
13	114	SLCT	I	SLCT	I
14	119	$\overline{AFD}$	I/O	$\overline{DSTRB}$	I/O
15	116	$\overline{ERR}$	I	$\overline{ERR}$	I
16	117	$\overline{INIT}$	I/O	$\overline{INIT}$	I/O
17	118	$\overline{SLIN}$	I/O	$\overline{ASTRB}$	I/O
18 - 23		GND		GND	
25		GND		GND	

7.0 UART1 and UART2 (with Fast IR) (Logical Devices 6 and 5)

This section describes the functionality of the Legacy UART (16450/16550), Enhanced UART and the IR modes.

UART1 supports standard 16450/16550 mode.

UART2 supports standard 16450/16550, Enhanced UART and Fast IR modes.

UART1 is a subset of UART2 functionality. It supports UART mode hard-wired communications, but does not support IR communication. Therefore, all explanations of IR communication in this section do not apply to UART1.

The UART module provides advanced, versatile serial communications features with infrared capabilities. It supports six modes of operation: UART, Sharp-IR, IrDA 1.0 SIR, IrDA 1.1 MIR, IrDA 1.1 FIR, and Consumer-IR (also called TV-Remote or Consumer remote-control). In this section, the IrDA modes are referred to by their abbreviated names. e.g. SIR, MIR and FIR. In UART mode, the module can function as a standard 16450 or 16550, or as an Extended UART.

Existing 16550-based legacy software is completely and transparently supported. Module organization and specific fallback mechanisms switch the module to 16550 compatibility mode upon reset or when initialized by 16550 software.

The module includes two DMA channels that can support all operational modes. The device can use either 1 or 2 DMA channels. One channel is required for infrared based applications since infrared communications work in half duplex fashion. Two channels would normally be needed to handle high-speed full duplex UART based applications.

The module includes a 12-bit 125 µsec resolution timer that simplifies driver design and infrared communications protocol implementation.

7.1 FEATURES

- Fully compatible with 16550A and 16450 devices
- Automatic fallback to 16550A compatibility mode
- Extended UART mode
- UART baud rates up to 1.5 Mbps
- Sharp-IR with selectable internal or external modulation/demodulation
- IrDA 1.0 SIR with data rates up to 115.2 Kbps
- IrDA 1.1 MIR and FIR with data rates of 0.576, 1.152 and 4.0 Mbps
- Consumer-IR (TV-Remote) mode
- Back-to-back infrared frame transmission and reception
- Full duplex infrared capability for diagnostics
- Transmission deferral (in fast IR modes)
- IrDA modes pipelining
- Selectable 16 or 32-level transmission and reception FIFOs (RX_FIFO & TX_FIFO respectively)
- 8-level ST_FIFO (ST_FIFO)
- Multiple optical transceiver support
- Automatic or manual transceiver configuration
- 12-bit timer for infrared protocol support
- Support for Plug-n-Play infrared adapters

7.2 FUNCTIONAL MODES OVERVIEW

This multi-mode module can be configured to act as any one of several different functions. Although each mode is unique, certain system resources and features are common to some or to all modes.

7.2.1 UART Modes: 16450 or 16550, and Extended

UART modes support serial data communications with a remote peripheral device or modem using a wired interface. The device transmits and receives data concurrently in full-duplex operation, performing parallel-to-serial and serial-to-parallel conversion and other functions required to exchange parallel data with the system. It also interfaces with external devices using a programmable serial communications format.

The following UART modes are supported:

- 16450 or 16550 mode (Non-Extended modes)
- Extended mode

The 16450 or 16550 mode is functionally and software-compatible with the standard 16450 or 16550 UARTs. This is the default mode of operation after power up, after reset or when initialized by software written for the 16450 or 16550 UART (Special mechanisms switch the module automatically to 16550 UART mode when standard 16550 software is run).

The 16550 UART mode has all the features of the 16450 mode, with the addition of 16-byte data FIFOs for more efficient data I/O.

In Extended mode, additional features become available that enhance the UART performance, such as timer access, additional interrupts and DMA ability (see ”Extended UART Mode” on page 110).

The UART supports baud rates of up to 115.2 Kbps in 16450 or 16550 mode, and up to 1.5 Mbps in Extended mode.

7.2.2 Sharp-IR, IrDA SIR Infrared Modes

The Sharp-IR mode provides bidirectional communication by transmitting and receiving infrared radiation. In this mode, infrared I/O circuits was added to the UART, which operates at 38.4 Kbps in half-duplex, using normal UART serial data formats with Digital Amplitude Shift Keying (DASK) modulation. The modulation/demodulation can be operated internally or externally.

In SIR mode, the system functions similarly to the Sharp-IR mode, but at 115.2 Kbps.

7.2.3 High Speed Infrared Modes: IrDA MIR, FIR

The infrared support of this module includes both IrDA 1.1 MIR and FIR modes, with data rates of 567 Kbps, 1.152 Mbps and 4.0 Mbps. The data format differs from the previous infrared modes. Those modes relay word-oriented data formats produced by the UART via infrared I/O circuits. In the fast infrared modes, a frame-oriented serial format is

employed instead of word-oriented. These changes enable more efficient channel data bandwidth utilization and more effective error detection/correction.

7.2.4 Consumer IR Mode

Consumer-IR mode supports all the protocols presently used in remote-controlled home entertainment equipment: RC-5, RC-6, RECS 80, NEC and RCA. Like the high-speed IR modes, the serial format is not compatible with UART operation, and specific circuitry performs all the hardware tasks required for signal conditioning and formatting. The software is responsible for the generation of the infrared code to be transmitted, and for the interpretation of the received code.

7.3 REGISTER BANK OVERVIEW

Eight register banks, each containing eight registers, control UART operation. All registers use the same 8-byte address space to indicate offsets 00h through 07h, and the active bank must be selected by the software.

The register bank organization enables access to the banks as required for activation of all module modes, while maintaining transparent compatibility with 16450 or 16550 software, which activates only the registers and specific bits used in those devices. For details, See Section 7.4.

The Bank Selection Register (BSR) selects the active bank and is common to all banks. See Figure 7-1. Therefore, each bank defines seven new registers.

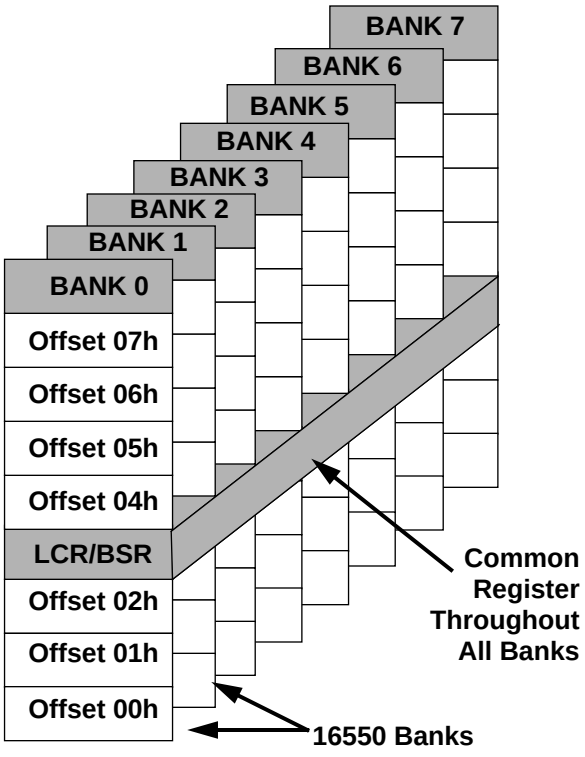


FIGURE 7-1. Register Bank Architecture

The default bank selection after system reset is 0, which places the module in the UART 16550 mode. Additionally, setting the baud rate in bank 1 (as required to initialize the 16550 UART) switches the module to a Non-Extended UART mode. This ensures that running existing 16550 software will switch the system to the 16550 configuration without software modification.

Table 7-1 shows the main functions of the registers in each bank. Banks 0-3 control both UART and infrared modes of operation; banks 4-7 control and configure the infrared modes only.

TABLE 7-1. Register Bank Summary

Bank	UART	IR Mode	Main Functions
0	✓	✓	Global Control and Status
1	✓	✓	Legacy Bank
2	✓	✓	Baud Rate Generator Divisor, Extended Control and Status
3	✓	✓	Module Revision ID and Shadow Registers
4		✓	Timer and Counters
5		✓	Infrared Control and ST_FIFO
6		✓	Infrared Physical Layer Configuration
7		✓	Consumer-IR and Optical Transceiver Configuration

Banks 0 and 1 are the 16550 register banks. The registers in these banks are equivalent to the registers contained in the 16550 UARTs and are accessed by 16550 software drivers as if the module was a 16550. Bank 1 contains the baud rate divisor ports. Bank 0 registers control all other aspects of the UART function, including data transfers, format setup parameters, interrupt setup and status monitoring.

Bank 2 ccontains the non-legacy Baud Rate Generator Divisor ports, and controls the extended features special to this UART that are not included in the 16550 repertoire. These include DMA and timer usage. See ”Extended UART Mode” on page 110.

Bank 3 contains the Module Revision ID and shadow registers. The Module Revision ID (MRID) register contains a code that identifies the revision of the module when read by software. The shadow registers contain the identical content as reset-when-read registers within bank 0. Reading their contents from the shadow registers lets the system read the register content without resetting them.

Bank 4 contains counter and timer access registers. The 12-bit timer may be used by the UART in Extended mode, or by the infrared modes. The counters are used by the fast infrared modes which communicate in frame-oriented formats and need to count frame lengths for control.

Bank 5 registers control infrared parameters related to the logical system I/O parameters, and the ST_FIFO used in fast infrared communications.

Bank 6 registers control physical characteristics involved in infrared communications (e.g. pulse width selection).

Bank 7 registers are dedicated to Consumer-IR configuration and control.

7.4 UART MODES – DETAILED DESCRIPTION

The UART modes support serial data communications with a remote peripheral device or modem using a wired interface.

The module provides receive and transmit channels that can operate concurrently in full-duplex mode. This module performs all functions required to conduct parallel data interchange with the system and composite serial data exchange with the external data channel, including:

- Format conversion between the internal parallel data format and the external programmable composite serial format. See Figure 7-2.
- Serial data timing generation and recognition
- Parallel data interchange with the system using a choice of bi-directional data transfer mechanisms
- Status monitoring for all phases of the communications activity

The module supplies modem control registers, and a prioritized interrupt system for efficient interrupt handling.

7.4.1 16450 or 16550 UART Mode

The module defaults to 16450 mode after power up or reset. UART 16550 mode is equivalent to 16450 mode, with the addition of a 16-byte data FIFO for more efficient data I/O. Transparent compatibility is preserved with this UART mode in this module.

Despite the many additions to the basic UART hardware and organization, the UART responds correctly to existing software drivers with no software modification required. When 16450 software initializes and addresses this module, it will in always perform as a 16450 device.

Data transfer takes place by use of data buffers that interface internally in parallel and with the external data channel in a serial format. 16-byte data FIFOs may reduce host overhead by enabling multiple-byte data transfers within a single interrupt. With FIFOs disabled, this module is equivalent to the standard 16450 UART. With FIFOs enabled, the hardware functions as a standard 16550 UART.

The composite serial data stream interfaces with the data channel through signal conditioning circuitry such as TTL/RS232 converters, modem tone generators, etc.

Data transfer is accompanied by software-generated control signals, which may be utilized to activate the communications channel and “handshake” with the remote device. These may be supplied directly by the UART, or generated by control interface circuits such as telephone dialing and answering circuits, etc.

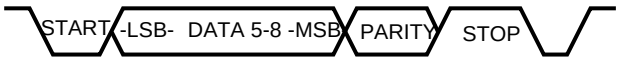


FIGURE 7-2. Composite Serial Data

The composite serial data stream produced by the UART is illustrated in Figure 7-2. A data word containing five to eight bits is preceded by start bits and followed by an optional parity bit and a stop bit. The data is clocked out, LSB first, at a predetermined rate (the baud rate).

The data word length, parity bit option, number of start bits and baud rate are programmable parameters.

The UART includes a programmable baud rate generator that produces the baud rate clocks and associated timing signals for serial communication.

The system can monitor this module status at any time. Status information includes the type and condition of the transfer operation in process, as well as any error conditions (e.g., parity, overrun, framing, or break interrupt).

The module resources include modem control capability and a prioritized interrupt system. Interrupts can be programmed to match system requirements, minimizing the CPU overhead required to handle the communications link.

Programmable Baud Rate Generator

This module contains a programmable baud rate generator that generates the clock rates for serial data communication (both transmit and receive channels). It divides its input clock by any divisor value from 1 to 2^{16} - 1. The output clock frequency of the baud rate generator must be programmed to be sixteen times the baud rate value. A 24 MHz input frequency is divided by a prescale value (PRESL field of EXCR2 - see page 132. Its default value is 13) and by a 16-bit programmable divisor value contained in the Baud Rate Generator Divisor High and Low registers (BGD(H) and BGD(L) - see page 129). Each divisor value yields a clock signal (BOUT) and a further division by 16 produces the baud rate clock for the serial data stream. It may also be output as a test signal when enabled (see bit 7 of EXCR1 on page 130.)

These user-selectable parameters enable the user to generate a large choice of serial data rates, including all standard baud rates. A list of baud rates and their settings appears in Table 7-14 on page 130.

Module Operation

Before module operation can begin, both the communications format and baud rate must be programmed by the software. The communications format is programmed by loading a control byte into the LCR register, while the baud rate is selected by loading an appropriate value into the baud rate generator divisor registers and the divisor preselect values (PRESL) into EXCR2 (see page 132).

The software can read the status of the module at any time during operation. The status information includes full or empty state for both transmission and reception channels, and any other condition detected on the received data stream, like parity error, framing error, data overrun, or break event.

7.4.2 Extended UART Mode

In Extended UART mode of operation, the module configuration changes and additional features become available which enhance UART capabilities.

- The interrupt sources are no longer prioritized; they are presented bit-by-bit in the EIR (see page 119).
- An auxiliary status and control register replaces the scratchpad register. It contains additional status and control flag bits (”Auxiliary Status and Control Register (ASCR), Bank 0, Offset 07h” on page 127).

- The TX_FIFO can generate interrupts when the number of outgoing bytes in the TX_FIFO drops below a programmable threshold. In the Non-Extended UART modes, only reception FIFOs have the thresholding feature.
- DMA capability is available.
- Interrupts occur when the transmitter becomes empty or a DMA event occurs.

7.5 SHARP-IR MODE – DETAILED DESCRIPTION

This mode supports bidirectional data communication with a remote device using infrared radiation as the transmission medium. Sharp-IR uses Digital Amplitude Shift Keying (DASK) and allows serial communication at baud rates up to 38.4 Kbaud. The format of the serial data is similar to the UART data format. Each data word is sent serially beginning with a zero value start bit, followed by up to eight data bits (LSB first), an optional parity bit, and ending with at least one stop bit with a binary value of one. A logical zero is signalled by sending a 500 KHz continuous pulse train of infrared radiation. A logical 1 is signalled by the absence of any infrared signal. This module can perform the modulation and demodulation operations internally, or can rely on the external optical module to perform them.

Sharp-IR device operation is similar to the operation in UART modes, the main difference being that data transfer operations are normally performed in half duplex fashion, and the modem control and status signals are not used. Selection of the Sharp-IR mode is controlled by the Mode Select (MDSL) bits in the MCR register when the module is in Extended mode, or by the IR_SL bits in the IRCR1 register when the module is not in extended mode. This prevents legacy software, running in non-extended mode, from spuriously switching the module to UART mode, when the software writes to the MCR register.

7.6 SIR MODE – DETAILED DESCRIPTION

This operational mode supports bidirectional data communication with a remote device using infrared radiation as the transmission medium.

SIR allows serial communication at baud rates up to 115.2 Kbuad. The serial data format is similar to the UART data format. Each data word is sent serially beginning with a 0 value start bit, followed by eight data bits (LSB first), an optional parity bit, and ending with at least one stop bit with a binary value of 1.

A zero value is signalled by sending a single infrared pulse. A one value is signalled by not sending any pulse. The width of each pulse can be either 1.6 µsec or 3/16 of the time required to transmit a single bit. (1.6 µsec equals 3/16 of the time required to transmit a single bit at 115.2 Kbps). This way, each word begins with a pulse for the start bit.

The module operation in SIR is similar to the operation in UART modes, the main difference being that data transfer operations are normally performed in half duplex fashion. Selection of the IrDA 1.0 SIR mode is controlled by the MDSL bits in the MCR register when the UART is in Extended mode, or by the IR_SL bits in the IRCR1 register when the UART is not in Extended mode. This prevents legacy software, running in Non-Extended mode, from spuriously switching the module to UART mode, when the software writes to the MCR register.

7.7 MIR AND FIR MODES – DETAILED DESCRIPTION

This module supports both IrDA 1.1 MIR and FIR modes, with data rates of 576 Kbps, 1.152 Mbps and 4.0 Mbps.

These high-speed modes differ from the previous communications modes in that the communication is now frame-oriented rather than word-oriented. Details on the frame format, encoding schemes, CRC sequences, etc. are provided in the appropriate IrDA documents. These modes do not use the same serial word formats as the UART modes; they generate complete frames of data which can be transferred faster, more efficiently and with more sophisticated error detection or correction than word-oriented transmission.

The MIR transmitter's front end performs bit stuffing on the outbound data stream and places start and stop flags at the beginning and end of MIR frames. The MIR receiver's front-end removes flags and "de-stuffs" the inbound bit stream, and checks for abort conditions.

The FIR transmitter's front end adds a preamble as well as start and stop flags to each frame, and encodes the transmission data into a 4 ppm (Pulse Position Modulation) data stream. The FIR receiver's front end strips the preamble and flags from the inbound data stream and decodes the 4 ppm data, while also checking for coding violations.

Both MIR and FIR front ends also automatically append CRC sequences to transmitted frames and check for CRC errors on received frames.

7.7.1 High-Speed Infrared Transmission

Transmission of a frame begins when the CPU or the DMA controller writes data into the TX_FIFO while it is empty.

Frame transmission can be completed normally by using one of the following methods:

- S_EOT bit (Set End of Transmission), bit 2 in ASCR Register, in Bank 0 Offset 07h.

  This method is used when data transfers are performed in Programmed I/O (PIO) mode. When the CPU sets the S_EOT bit before writing the last byte into the TX_FIFO, the byte is tagged with an End-Of-Frame (EOF) indication. When this byte reaches the TX_FIFO bottom, and is read by the transmitter front end, a CRC is appended to the transmitted data and the frame is normally terminated.

- DMA TC signal (DMA Terminal Count)

  This method is used when data transfers are performed in DMA mode. It works similarly to the previous method except that the tagging of the last byte of a frame occurs when the DMA controller asserts the TC signal during a write of the last byte to the TX_FIFO.

- Frame Length Counter

  This method can be used when data transfers are performed in either PIO or DMA mode. The value of the FEND_MD bit in the IRCR2 register determines whether the Frame Length Counter is effective in the PIO or DMA mode.

  The counter is loaded from the frame length register (TFRL) at the beginning of each frame, and is decremented as each byte is transmitted. An EOF is generated when the counter reaches zero. When used in DMA mode with an 8237 type DMA controller, if the block size is not an exact multiple of the frame size, this method allows a large data block to be automatically split into

equal-size back-to-back frames, plus a shorter frame that is terminated by the DMA TC signal if the block size is not an exact multiple of the frame size.

An option is also provided to stop transmission at the end of each frame. This happens when the transmitter frame-end stop mode is selected (TX_MS bit in IRCR2 register set to 1).

By using this option, the software can send frames of different sizes without re-initializing the DMA controller for each frame. After transmission of each frame, the transmitter stops and generates an interrupt. The software loads the length of the next frame into the TFRL register and restarts the transmitter by clearing the TXHFE bit in the ASCR register.

Note: PIO or DMA mode is controlled by setting the DMA_EN bit in the extended-mode MCR register. DMA cycles always access the Transmission or RX_FIFO, regardless of the selected bank. In PIO mode, Bank 0 must be selected to enable CPU access to the FIFOs. When DMA_EN is set to 1 (DMA enabled) the CPU may access the RX_FIFO and the TX_FIFO, but these accesses will be treated as DMA accesses as far as the function of the FEND_MD bit in the IRCR2 (see page 138) is concerned.

Underrun Event Description

While a frame is being transmitted, data must be written to the TX_FIFO at a rate dictated by the transmission speed. If the CPU or DMA controller fails to meet this requirement, a transmitter underrun occurs, an inverted CRC is appended to the frame being transmitted, and the frame is terminated with a stop flag. Data transmission then stops. Transmission of the inverted CRC ensures that the remote receiving device will receive the frame with a CRC error and will discard it.

Following an underrun condition, data transmission always stops at the next frame boundary. The frame bytes from the point where the underrun occurred to the end of the frame are not sent out to the external infrared interface. Nonetheless, they are removed from the TX_FIFO by the transmitter and discarded. The underrun indication is reported only when the transmitter detects the end of frame via one of the methods described above.

The software can do various things to recover from an underrun condition. For example, the software can simply clear the underrun condition by writing a 1 into bit 6 of ASCR and retransmit the underrun frame later, or it can retransmit the underrun frame immediately, before transmitting other frames.

If the software chooses to retransmit the frame immediately, it must perform the following steps:

1. Disable DMA, if DMA mode was selected.
2. Read the TXFLV register to determine the number of bytes in the TX_FIFO.(This is needed to determine the exact point where the underrun occurred, and whether or not the first byte of a new frame is in the TX_FIFO).
3. Reset the TX_FIFO.
4. Backup DMA controller registers.
5. Clear the transmission underrun bit.
6. Re-enable DMA controller.

7.7.2 High Speed Infrared Reception

When the receiver's front end detects an incoming frame, it starts de-serializing the infrared bit stream and loads the resulting data bytes into the RX_FIFO. When the EOF is detected, two or four CRC bytes are appended to the received data, and an EOF flag is written into the tag section of the RX_FIFO along with the last byte. In the present implementation, the CRC bytes are always transferred to the RX_FIFO following the data.

Additional status information, related to the received frame, is also written into the RX_FIFO tag section along with the last byte. The status information will be loaded into the LSR register when the last frame byte reaches the bottom of the RX_FIFO. The receiver counts received bytes from the beginning of the current frame, and will only transfer to the RX_FIFO a number of bytes not exceeding the max frame length value (programmed via the RFRML register in bank 4). If any additional frame bytes are present they are discarded and the MAX_LEN error flag is set.

Although data can be transferred from the RX_FIFO to memory in either PIO or DMA mode, DMA mode should be used due to the high data rates.

An eight-level **ST_FIFO** is provided to handle back-to-back incoming frames, when DMA mode is selected and an 8237 type DMA controller is used.

When an End-Of-Frame (EOF) mark is detected in 8237 DMA mode, the status and byte count information for the frame is written into the ST_FIFO. An interrupt is also generated when the ST_FIFO level reaches a programmed threshold or a ST_FIFO time-out occurs.

The CPU uses this information to locate the frame boundaries in the memory buffer where data belonging to several received frames has been transferred by the 8237 type DMA controller.

The ST_FIFO and the received frame length can be used to determine the validity and the position of the received frames inside the reception buffer.

If the RX_FIFO and/or the ST_FIFO fills up during multiple frames reception due to the DMA controller or CPU not serving them in time, data frames might be crushed and lost. This means that no bytes belonging to these frames were written to the RX_FIFO. In fact, a frame will be lost in 8237 DMA mode when the ST_FIFO is full for the entire time during which the frame is being received, even though there were empty locations in the RX_FIFO. This is because no data bytes can be loaded into the RX_FIFO, and then transferred to memory by the DMA controller, unless there is at least one available entry in the ST_FIFO to store the number of received bytes. This information, as mentioned before, is needed by the software to locate the frame boundaries in the DMA memory buffer.

In the event that a number of frames are lost, for any of the reasons mentioned above, one or more lost-frame indications including the number of lost frames, are loaded into the ST_FIFO.

Frames can also be lost in PIO mode , but only when the RX_FIFO is full. The reason for that, in these cases, is that the ST_FIFO stores only lost-frame indications, not frame status or byte counts.

7.8 CONSUMER-IR MODE – DETAILED DESCRIPTION

The Consumer-IR circuitry in this module is designed to optimally support all the major protocols presently used in remote-controlled home entertainment equipment: RC-5, RC-6, RECS 80, NEC and RCA.

This module, in conjunction with an external optical device, provides the physical layer functions necessary to support these protocols. These functions include: modulation, demodulation, serialization, deserialization, data buffering, status reporting, interrupt generation, etc.

The software is responsible for the generation of the infrared code to be transmitted, and for the interpretation of the received code.

7.8.1 Consumer-IR Transmission

The code to be transmitted consists of a sequence of bytes that represent either a bit string or a set of run-length codes. The number of bits or run-length codes usually needed to represent each infrared code bit depends on the infrared protocol to be used. The RC-5 protocol, for example, needs two bits or between one and two run-length codes to represent each infrared code bit.

Transmission is initiated when the CPU or DMA module writes code bytes into the empty TX_FIFO. Transmission is normally completed when the CPU sets the S_EOT bit in the ASCR register (See Section 7.13.10 on page 127), before writing the last byte, or when the DMA controller activates the TC (terminal count) signal. Transmission will also terminate if the CPU simply stops transferring data and the transmitter becomes empty. In this case, however, a transmitter-underrun condition will be generated, which must be cleared in order to begin the next transmission.

The transmission bytes are either de-serialized or run-length encoded, and the resulting bit string modulates a carrier signal and is sent to the transmitter LED. The transfer rate of this bit string, like in the UART modes, is determined by the value programmed in the baud rate generator divisor registers. Unlike a UART transmission, start, stop and parity bits are not included in the transmitted data stream. A logic 1 in the bit string keeps the LED off, so no infrared signal is transmitted. A logic 0, generates a sequence of modulating pulses which will turn on the transmitter LED. Frequency and pulse width of the modulating pulses are programmed by the MCFR and MCPW fields in the IRTXMC register as well as the TXHSC bit in the RCCFG register. Sections 7.20.2 and 7.20.3 describe these registers in detail.

The RC_MMD field selects the transmitter modulation mode. If C_PLS mode is selected, modulating pulses are generated continuously for the entire logic 0 bit time. If 6_PLS or 8_PLS mode is selected, six or eight pulses are generated each time a logic 0 bit is transmitted following a logic 1 bit. The total transmission time for the logic 0 bits must be equal-to or greater-than 6 or 8 times the period of the modulation subcarrier, otherwise, fewer pulses will be transmitted.

C_PLS modulation mode is used for RC-5, RC-6, NEC and RCA protocols. 8_PLS or 6_PLS modulation mode is used for the RECS 80 protocol. The 8_PLS or 6_PLS mode allows minimization of the number of bits needed to represent the RECS 80 infrared code sequence. The current transmitter implementation supports only the modulated modes of the RECS 80 protocol. It does not support Flash mode.

7.8.2 Consumer-IR Reception

The Consumer-IR receiver is significantly different from a UART receiver in two ways. Firstly, the incoming infrared signals are DASK modulated. Therefore, demodulation may be necessary. Secondly, there are no start bits in the incoming data stream.

Whenever an infrared signal is detected, receiver operations depend on whether or not receiver demodulation is enabled. If demodulation is disabled, the receiver immediately becomes active. If demodulation is enabled, the receiver checks the carrier frequency of the incoming signal, and becomes active only if the frequency is within the programmed range. Otherwise, the signal is ignored and no other action is taken.

When the receiver enters the active state, the RXACT bit in the ASCR register is set to 1. Once in the active state, the receiver keeps sampling the infrared input signal and generates a bit string where a logic 1 indicates an idle condition and a logic 0 indicates the presence of infrared energy. The infrared input is sampled regardless of the presence of infrared pulses at a rate determined by the value loaded into the baud rate generator divisor registers. The received bit string is either de-serialized and assembled into 8-bit characters, or it is converted to run-length encoded values. The resulting data bytes are then transferred into the RX_FIFO.

The receiver also sets the RXWDG bit in the ASCR register each time an infrared pulse signal is detected. This bit is automatically cleared when the ASCR register is read, and it is intended to assist the software in determining when the infrared link has been idle for a certain time. The software can then stop the data reception by writing a 1 into the RXACT bit to clear it and return the receiver to the inactive state.

The frequency bandwidth for the incoming modulated infrared signal is selected by the DFR and DBW fields in the IRRXDC register.

There are two Consumer-IR reception data modes: “Over-sampled” and “Programmed T Period” mode. For either mode the sampling rate is determined by the setting of the baud rate generator divisor registers.

The “Over-sampled” mode can be used with the receiver demodulator either enabled or disabled. It should be used with the demodulator disabled when a detailed snapshot of the incoming signal is needed, for example to determine the period of the carrier signal. If the demodulator is enabled, the stream of samples can be used to reconstruct the incoming bit string. To obtain good resolution, a fairly high sampling rate should be selected.

The “Programmed-T-Period” mode should be used with the receiver demodulator enabled. The T Period represents one half bit time for protocols using biphase encoding, or the basic unit of pulse distance for protocols using pulse distance encoding. The baud rate is usually programmed to match the T Period. For long periods of logic low or high, the receiver samples the demodulated signal at the programmed sampling rate.

Whenever a new infrared energy pulse is detected, the receiver synchronizes the sampling process to the incoming signal timing. This reduces timing related errors and eliminates the possibility of missing short infrared pulse sequences, especially with the RECS 80 protocol.

In addition, the “Programmed-T-Period” sampling minimizes the amount of data used to represent the incoming infrared signal, therefore reducing the processing overhead in the host CPU.

7.9 FIFO TIME-OUTS

Time-out mechanisms prevent received data from remaining in the RX_FIFO and/or the ST_FIFO indefinitely, if the programmed interrupt or DMA thresholds are not reached.

An RX_FIFO time-out generates a Receiver Data Ready interrupt and/or a receiver DMA request if bit 0 of IER and/or bit 2 of MCR (in Extended mode) are set to 1 respectively. An RX_FIFO time-out also sets bit 0 of ASCR to 1 if the RX_FIFO is below the threshold. When a Receiver Data Ready interrupt occurs, this bit is tested by the software to determine whether a number of bytes indicated by the RX_FIFO threshold can be read without checking bit 0 of the LSR register.

A ST_FIFO time-out is enabled only in MIR and FIR modes, and generates an interrupt if bit 6 of IER is set to 1.

The conditions that must exist for a time-out to occur in the various modes of operation are described below.

When a time-out has occurred, it can only be reset when the FIFO is read by the CPU or DMA controller.

7.9.1 MIR or FIR Mode Time-Out Conditions

An RX_FIFO time-out occurs when all of the following are true:

- At least one byte is in the RX_FIFO

and

- More than 64 µsec have elapsed since the last byte was loaded into the RX_FIFO from the receiver logic

and

- More than 64 µsec have elapsed since the last byte was read from the RX_FIFO by the CPU or DMA controller.

An ST_FIFO time-out occurs when all of the following are true:

- At least one entry is in the ST_FIFO

and

- More than 1 msec has elapsed since the last entry was loaded into the RX_FIFO by the receiver logic

and

- More than 1 msec has elapsed since the last entry was read from the ST_FIFO by the CPU.

7.9.2 UART, SIR or Sharp-IR Mode Time-Out Conditions

Two timers (timer1 and timer 2) are used to generate two different time-out events (A and B, respectively). Timer 1 times out after 64 µsec. Timer 2 times out after four character times.

Time-out event A generates an interrupt and sets the RXF_TOUT bit (bit 0 of ASCR) when all of the following are true:

- At least one byte is in the RX_FIFO, and
- More than 64 µsec or four character times, whichever is greater, have elapsed since the last byte was loaded into the RX_FIFO from the receiver logic, and
- More than 64 µsec or four character times, whichever is greater, have elapsed since the last byte was read from the RX_FIFO by the CPU or DMA controller.

Time-out event B activates the receiver DMA request and is invisible to the software. It occurs when all of the following are true:

- At least one byte is in the RX_FIFO, and
- More than 64 µsec or four character times, whichever is smaller, have elapsed since the last byte was loaded into the RX_FIFO from the receiver logic, and
- More than 64 µsec or four character times, whichever is smaller, have elapsed since the last byte was read from the RX_FIFO by the CPU or DMA controller.

7.9.3 Consumer-IR Mode Time-Out Conditions

The RX_FIFO time-out, in Consumer-IR mode, is disabled while the receiver is active. It occurs when all of the following are true:

- At least one byte has been in the RX_FIFO for 64 µsec or more, and
- The receiver has been inactive (RXACT = 0) for 64 µsec or more, and
- More than 64 µsec have elapsed since the last byte was read from the RX_FIFO by the CPU or DMA controller.

7.9.4 Transmission Deferral

This feature allows software to send short high-speed data frames in Programmed Input/Output (PIO) mode without the risk of generating a transmitter underrun .

Although this feature is available and works identically in all the Extended modes, its use will most likely be confined to MIR and FIR modes to support high-speed negotiation. (In other modes, either the relatively slow transmission data rate lets the CPU keep up without letting an underrun occur, as in the case of the Consumer-IR mode, or else transmission underrun s are allowed and are not considered to be error conditions.

Transmission deferral is available only in Extended mode and when the TX_FIFO is enabled. When transmission deferral is enabled (TX_DFR bit in the MCR register set to 1) and the transmitter becomes empty, an internal flag is set that locks the transmitter. If the CPU now writes data into the TX_FIFO, the transmitter does not start sending the data until the TX_FIFO level reaches either 14 for a 16-level TX_FIFO, or 30 for a 32-level TX_FIFO, at which time the internal flag is cleared. The internal flag is also cleared and the transmitter starts transmitting when a time-out condition is reached. This prevents some bytes from being in the TX_FIFO indefinitely if the threshold is not reached.

The time-out mechanism is implemented by a timer that is enabled when the internal flag is set and there is at least one byte in the TX_FIFO. Whenever a byte is loaded into the TX_FIFO the timer gets reloaded with the initial value. If no bytes are loaded for a 64-µsec time, the timer times out and the internal flag is cleared, thus enabling the transmitter.

7.10 AUTOMATIC FALLBACK TO A NON-EXTENDED UART MODE

The automatic fallback feature supports existing legacy software packages that use the 16550 UART by automatically turning off any Extended mode features and switches the UART to Non-Extended mode when either of the LBGD(L) or LBGD(H) ports in bank 1 is read from or written to by the CPU.

This eliminates the need for user intervention prior to running a legacy program.

In order to avoid spurious fallbacks, alternate baud rate registers are provided in bank 2. Any program designed to take advantage of the UART's extended features, should not use LBGD(L) and LBGD(H) to change the baud rate. It should use the BGD(L) and BGD(H) registers instead. Access to these ports will not cause fallback.

Fallback can occur in any mode. In Extended UART mode, fallback is always enabled. In this case, when a fallback occurs, the following happens:

- Transmission and Reception FIFOs switch to 16 levels.
- A value of 13 is selected for the baud rate generator prescaler
- The BTEST and ETDLBK bits in the EXCR1 register are cleared.
- UART mode is selected.
- A switch to a Non-Extended UART mode occurs.

When a fallback occurs in a Non-Extended UART mode, the last two of the above actions do not take place.

No switch to UART mode occurs if either SIR or Sharp-IR mode was selected. This prevents spurious switching to UART mode when a legacy program running in infrared mode accesses the baud rate generator divisor registers from bank 1.

Fallback from a Non-Extended mode can be disabled by setting the LOCK bit in register EXCR2. When LOCK is set to 1 and the UART is in a Non-Extended mode, two scratch registers overlaid with LBGD(L) and LBGD(H) are enabled. Any attempted CPU access of LBGD(L) and LBGD(H) accesses the scratch registers, and the baud rate setting is not affected. This feature allows existing legacy programs to run faster than 115.2 Kbps.

7.11 PIPELINING

When successive Infrared serial data streams must be communicated using the UART, the system can be pre-programmed to switch between different serial formats and different infrared modes by hardware, without software intervention during the process. This saves time and reduces system overhead. This automatic switching process between communication modes is called pipelining.

Pipelining minimizes the delay from the end of a negotiation phase to the subsequent data transfer phase in the IrDA infrared operation modes (SIR, MIR and FIR). The module does this by automatically selecting a new infrared operation mode and/or loading new values into the baud rate generator divisor registers as soon as the current data transmission completes and the transmitter becomes empty. The new operation mode and baud rate generator divisor values are programmed into special pipeline registers.

Pipelining is automatically disabled after a pipeline operation takes place. Software should enable pipelining again after the special pipeline registers are reloaded.

The only restriction on the pipelined operation modes is that they must be IrDA modes. Nevertheless, SIR mode will most likely be the first operation mode in a pipeline, since SIR is the operation mode used by the negotiation procedures in the presently defined IrDA protocols.

Following a pipeline operation, the transmitter will be halted for 250 µsec to allow the newly selected receiver filter in the remote optical transceiver to stabilize.

If a switch from either MIR or FIR to SIR operation mode occurs as a result of pipelining, and the transmitter sent an infrared interaction pulse just before the mode switch, assertion of the transmitter DMA request signal is delayed by a character time (at the newly selected baud rate) or for 250 µsec, whichever is greater. This prevents transmission of the next SIR operation mode data from starting before completion of reception at the remote station of the character triggered by the interaction pulse.

Since pipelining occurs without software intervention, automatic transceiver configuration must be enabled.

7.12 OPTICAL TRANSCEIVER INTERFACE

This module implements a flexible interface for the external infrared transceiver. Several signals are provided for this purpose. A transceiver module with one or two reception signals, or two transceiver modules can interface directly with this module without any additional logic.

Since various operational modes are supported by this module, the transmitter power as well as the receiver filter in the transceiver module must be configured according to the selected mode.

This module provides four interface pins to control the infrared transceiver. ID/IRSL(2-0) are three I/O pins and ID3 is an Input pin. All of these pins are powered up as inputs.

When in input mode, they can be used to read the identification data of Plug-n-Play infrared adapters.

When in output mode, the logic levels of IRSL(2-0) can be either controlled directly by the software by setting bits 2-0 of the IRCFG1 register, or they can be automatically selected by this module whenever the operation mode changes.

The automatic transceiver configuration is enabled by setting the AMCFG bit (bit 7) in the IRCFG4 register to 1. It allows the low-level functional details of the transceiver module being used to be hidden from the software drivers. It also speeds up the transceiver mode selection and must be enabled if the pipelining feature is to be used.

The operation mode settings for the automatic configuration are determined by various bit fields in the Infrared Interface Configuration registers (IRCFG[4-1]) that must be programmed when the UART is initialized.

The ID0/IRSL0/IRRX2 pin can also be used as an input to support an additional infrared reception signal. In this case, however, only two configuration pins are available.

The IRSL0_DS and IRSL21_DS bits in the IRCFG4 register determines the direction of IRSL(2-0).

7.13 BANK 0 – GLOBAL CONTROL AND STATUS REGISTERS

In the Non-Extended modes of operation, bank 0 is compatible with both the 16450 and the 16550. Upon reset, this module defaults to the 16450 mode. In the Extended mode, all the Registers (except RXD/ TXD) offer additional features.

TABLE 7-2. Bank 0 Serial Controller Base Registers

Offset	Register Name	Description
00h	RXD/ TXD	Receiver Data Port/ Transmitter Data Port
01h	IER	Interrupt Enable Register
02h	EIR/ FCR	Event Identification Register/ FIFO Control Register
03h	LCR/ BSR	Link Control Register/ Bank Select Register
04h	MCR	Modem Control Register
05h	LSR	Link Status Register
06h	MSR	Modem Status Register
07h	SCR/ ASCR	Scratch Register/ Auxiliary Status and Control Register

7.13.1 Receiver Data Port (RXD) or the Transmitter Data Port (TXD), Bank 0, Offset 00h

These ports share the same address.

RXD is accessed during CPU read cycles. It is used to read data from the Receiver Holding Register when the FIFOs are disabled, or from the bottom of the RX_FIFO when the FIFOs are enabled. See Figure 7-3.

TXD is accessed during CPU write cycles. It is used to write data to the Transmitter Holding Register when the FIFOs are disabled, or to the TX_FIFO when the FIFOs are enabled. See Figure 7-4.

DMA cycles always access the TXD and RXD ports, regardless of the selected bank.

Receiver Data Port (RXD), Bank 0, Offset 00h

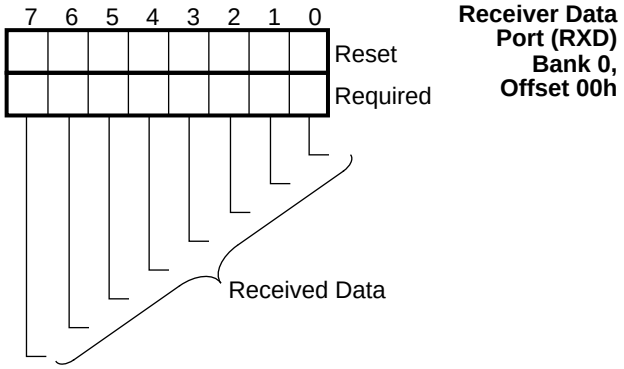


FIGURE 7-3. RXD Register Bitmap

Bits 7-0 - Received Data

Used to access the Receiver Holding Register when the FIFOs are disabled, or the bottom of the RX_FIFO when the FIFOs are enabled.

Transmitter Data Port (TXD), Bank 0, Offset 00h

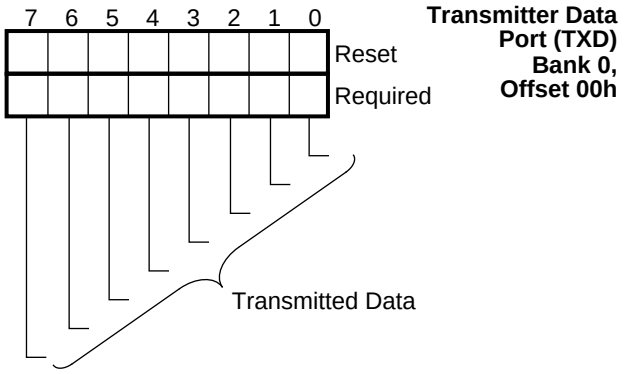


FIGURE 7-4. TXD Register Bitmap

Bits 7-0 - Transmitted Data

Used to access the Transmitter Holding Register when the FIFOs are disabled or the top of TX_FIFO when the FIFOs are enabled.

7.13.2 Interrupt Enable Register (IER), Bank 0, Offset 01h

This register controls the enabling of various interrupts. Some interrupts are common to all operating modes of the module, while others are mode specific. Bits 4 to 7 can be set in Extended mode only. They are cleared in Non-Extended mode. The bits of the Interrupt Enable Register (IER) are defined differently, depending on the operating mode of the module.

The different modes can be divided into the following five groups:

- Non-Extended (which includes UART, Sharp-IR and SIR).
- UART and Sharp-IR in Extended mode.
- SIR in Extended mode.
- Fast Infrared (MIR & FIR).
- Consumer-IR.

The following five sections describe the bits in this register for each of these modes.

The reset mode for the IER is the Non-Extended UART mode.

When edge-sensitive interrupt triggers are employed, user is advised to clear all IER bits immediately upon entering the interrupt service routine and to re-enable them prior to exiting (or alternatively, to disable CPU interrupts and re-enable prior to exiting). This will guarantee proper interrupt triggering in the interrupt controller in case one or more interrupt events occur during execution of the interrupt routine.

If the LSR, MSR or EIR registers are to be polled, interrupt sources which are identified by self-clearing bits should have their corresponding IER bits set to 0, to prevent spurious pulses on the interrupt output pin.

If an interrupt source must be disabled, the CPU can do so by clearing the corresponding bit in the IER register. However, if an interrupt event occurs just before the corresponding enable bit in the IER register is cleared, a spurious interrupt may be generated. To avoid this problem, the clearing of any IER bit should be done during execution of the interrupt service routine. If the interrupt controller is programmed for level-sensitive interrupts, the clearing of IER bits can also be performed outside the interrupt service routine, but with the CPU interrupt disabled.

Interrupt Enable Register (IER), in the Non-Extended Modes (UART, SIR and Sharp-IR)

Upon reset, the IER supports UART, SIR and Sharp-IR in the Non-Extended modes. Figure 7-5 shows the bitmap of the Interrupt Enable Register in these modes.

IER in Non-Extended Modes

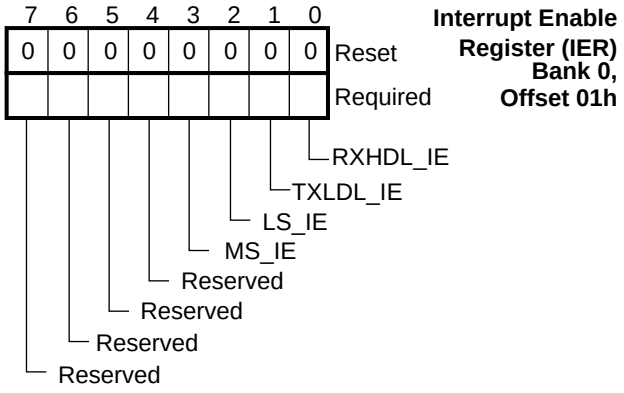


FIGURE 7-5. IER Register Bitmap, Non-Extended Mode

Bit 0 - Receiver High-Data-Level Interrupt Enable (RXHDL_IE)

Setting this bit enables interrupts on Receiver High-Data-Level, or RX_FIFO Time-Out events (EIR Bits 3-0 are 0100 or 1100. See ”Non-Extended Mode Interrupt Priorities” on page 120).

0 - Disable Receiver High-Data-Level and RX_FIFO Time-Out interrupts (Default).

1 - Enable Receiver High-Data-Level and RX_FIFO Time-Out interrupts.

Bit 1 - Transmitter Low-Data-Level Interrupt Enable (TXLDL_IE)

Setting this bit enables interrupts on Transmitter Low Data-Level-events (EIR Bits 3-0 are 0010. See ”Non-Extended Mode Interrupt Priorities” on page 120).

0 - Disable Transmitter Low-Data-Level Interrupts (Default).

1 - Enable Transmitter Low-Data-Level Interrupts.

Bit 2 - Link Status Interrupt Enable (LS_IE)

Setting this bit enables interrupts on Link Status events. (EIR Bits 3-0 are 0110. See ”Non-Extended Mode Interrupt Priorities” on page 120).

0 - Disable Link Status Interrupts (LS_EV) (Default).

1 - Enable Link Status Interrupts (LS_EV).

Bit 3 - Modem Status Interrupt Enable (MS_IE)

Setting this bit enables the interrupts on Modem Status events. (EIR Bits 3-0 are 0000. See ”Non-Extended Mode Interrupt Priorities” on page 120).

0 - Disable Modem Status Interrupts (MS_EV) (Default).

1 - Enable Modem Status Interrupts (MS_EV).

Bit 7-4- Reserved

These bits are reserved.

Interrupt Enable Register (IER), in the Extended Modes of UART and Sharp-IR

Figure 7-6 shows the bitmap of the Interrupt Enable Register in these modes.

Extended Mode of UART and Sharp-IR

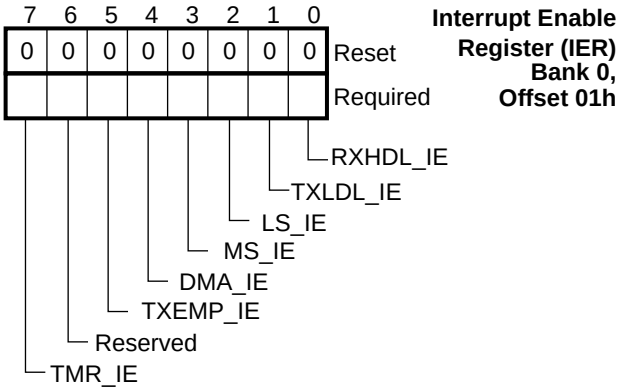


FIGURE 7-6. IER Register Bitmap, Extended Modes of UART and Sharp-IR

Bit 0 - Receiver High-Data-Level Interrupt Enable (RXHDL_IE)

Setting this bit enables interrupts when the RX_FIFO is equal to or above the RX_FIFO threshold level, or an RX_FIFO time out occurs.

0 - Disable Receiver Data Ready interrupt. (Default)

1 - Enable Receiver Data Ready interrupt.

Bit 1 - Transmitter Low-Data-Level Interrupt Enable (TXLDL_IE)

Setting this bit enables interrupts when the TX_FIFO is below the threshold level or the Transmitter Holding Register is empty.

0 - Disable Transmitter Low-Data-Level Interrupts (Default).

1 - Enable Transmitter Low-Data-Level Interrupts.

Bit 2 - Link Status Interrupt Enable (LS_IE)

Setting this bit enables interrupts on Link Status events.

0 - Disable Link Status Interrupts (LS_EV) (Default)

1 - Enable Link Status Interrupts (LS_EV).

Bit 3 - Modem Status Interrupt Enable (MS_IE)

Setting this bit enables the interrupts on Modem Status events.

0 - Disable Modem Status Interrupts (MS_EV) (Default)

1 - Enable Modem Status Interrupts (MS_EV).

Bit 4 - DMA Interrupt Enable (DMA_IE)

Setting this bit enables the interrupt on terminal count when the DMA is enabled.

0 - Disable DMA terminal count interrupt (Default)

1 - Enable DMA terminal count interrupt.

Bit 5 - Transmitter Empty Interrupt Enable (TXEMP_IE)

Setting this bit enables interrupt generation if the transmitter and TX_FIFO become empty.

0 - Disable Transmitter Empty interrupts (Default)

1 - Enable Transmitter Empty interrupts.

Bit 6 - Reserved

This bit is reserved.

Bit 7 - Timer Interrupt Enable (TMR_IE)

Setting this bit enables the timer interrupt.

0 - Disable Timer Interrupt (Default)

1 - Enable Timer Interrupt.

Interrupt Enable Register (IER), in the Extended Mode of SIR

Figure 7-7 shows the bitmap of the Interrupt Enable Register (IER) in this mode.

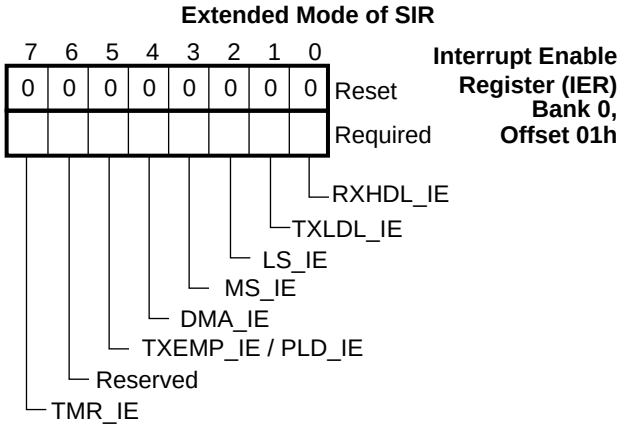


FIGURE 7-7. IER Register Bitmap, Extended Mode of SIR

Bit 4-0 -

Same as in the Extended Modes of UART and Sharp-IR (See previous section).

Bit 5 - Transmitter Empty Interrupt Enable (TXEMP_IE) and Pipeline Load Interrupt Enable (PLD_IE)

Enables interrupt generation if the transmitter becomes empty.

When pipeline mode is enabled, the transition from one mode to another is made upon the transmitter becoming empty.

0 - Disable Transmitter Empty and Pipeline Load interrupts (Default)

1 - Enable Transmitter Empty and Pipeline Load interrupts.

Bit 7-6 -

Same as in the Extended Modes of UART and Sharp-IR (See previous section).

Interrupt Enable Register (IER), Fast IR (MIR and FIR) Modes, Bank 0, Offset 01h

Figure 7-8 shows the bitmap of the Interrupt Enable Register in these modes.

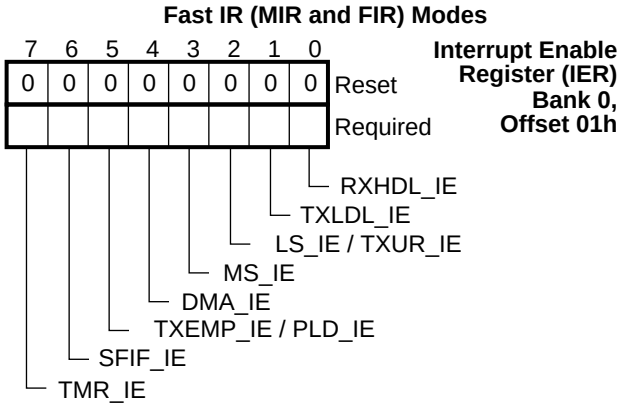


FIGURE 7-8. IER Register Bitmap, MIR and FIR Modes

Bit 1-0 -

Same as in the Extended Modes of UART and Sharp-IR (See previous sections).

Bit 2 - Link Status Interrupt Enable (LS_IE) or TX_FIFO Underrun Interrupt Enable (TXUR_IE)

On reception, Setting this bit enables Link Status Interrupts.

On transmission, Setting this bit enables TX_FIFO underrun interrupts.

0 - Disable Link Status and TX_FIFO underrun interrupts (Default)

1 - Enable Link Status and TX_FIFO underrun interrupts.

Bit 3 - Modem Status Interrupt Enable (MS_IE)

Setting this bit, when the IRMSSL bit in the IRCR2 register is cleared to 0, enables the modem status interrupts. Note that by default IRMSSL is set to 1 (See bit 2 of "Infrared Control Register 2 (IRCR2), Bank 5, Offset 04h" on page 138).

0 - Disable Modem Status Interrupts (MS_EV) (Default)

1 - Enable Modem Status Interrupts (MS_EV).

Bit 5-4 -

Same as in the Extended Modes of SIR (See previous section).

Bit 6 - ST_FIFO Threshold Interrupt Enable (SFIF_IE)

Setting this bit, enables interrupts when the ST_FIFO level is equal to or above the threshold. This interrupt is cleared when the ST_FIFO is read and its level drops below the threshold. (It is recomended to use this interrupt to service the ST_FIFO during back-to-back frame reception).

0 - Disable ST_FIFO Threshold Interrupts (Default)

1 - Enable ST_FIFO Threshold Interrupts (MS_EV).

Bit 7 -

Same as in the Extended Modes of SIR (See previous section).

Interrupt Enable Register (IER), Consumer-IR Mode, Bank 0, Offset 01h

Figure 7-9 shows the bitmap of the Interrupt Enable Register (IER) in this mode.

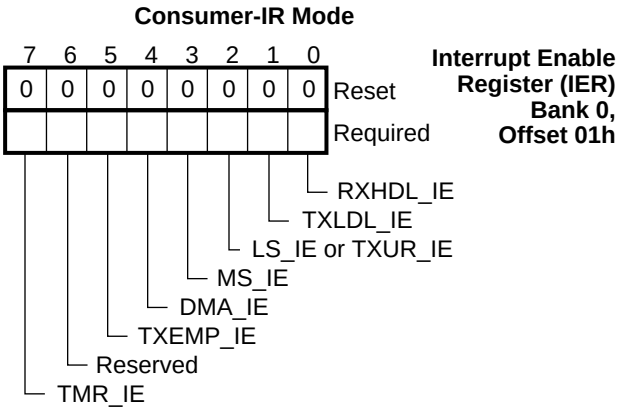


FIGURE 7-9. IER Register Bitmap, Consumer-IR Mode

Bit 4-0 -

Same as in the Fast IR (See previous section).

Bit 7-5 -

Same as in the Extended Modes of UART and Sharp-IR (See the section "Interrupt Enable Register (IER), in the Extended Modes of UART and Sharp-IR" on page 117).

7.13.3 Event Identification Register (EIR), Bank 0, Offset 02h

The **Event Identification Register (EIR)** and the **FIFO Control Register (FCR) (**see next register description) share the same address. The **EIR** is accessed during CPU read cycles while the **FCR** is accessed during CPU write cycles.The Event Identification Register (EIR) indicates the interrupt source. The function of this register changes according to the selected mode of operation.

Event Identification Register (EIR), Non-Extended Mode

When Extended mode is not selected (EXT_SL bit in EXCR1 register is set to 0), this register is the same as in the 16550.

In a Non-Extended UART mode, this module prioritizes interrupts into four levels. The EIR indicates the highest level of interrupt that is pending. The encoding of these interrupts is shown in Table 7-3.

When the EIR is being read, the display of the highest priority pending interrupt is frozen; new interrupt requests are recorded, but the indication is not updated until the access is complete.

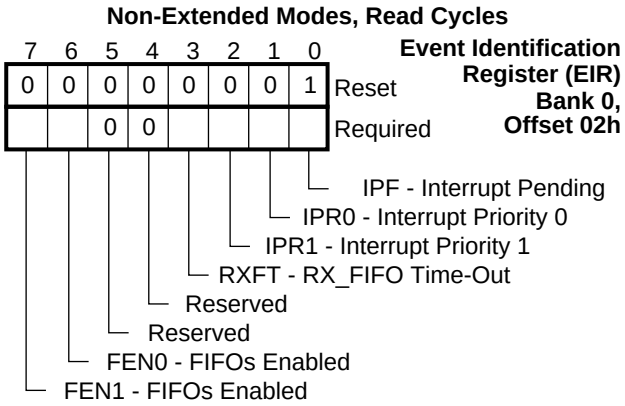


FIGURE 7-10. EIR Register Bitmap, Non-Extended Modes

Bit 0 - Interrupt Pending Flag (IPF)

0 - There is an interrupt pending.

1 - No interrupt pending. (Default)

Bits 2,1 - Interrupt Priority 1,0 (IPR1,0)

When bit 0 (IPF) is 0, these bits indicate the pending interrupt with the highest priority. See Table 7-3.

Default value is 00.

Bits 3 - RX_FIFO Time-Out (RXFT)

In the 16450 mode, this bit is always 0. In the 16550 mode (FIFOs enabled), this bit is set to 1 when an RX_FIFO read time-out occurred and the associated interrupt is currently the highest priority pending interrupt.

Bits 5,4 - Reserved

Read/Write 0.

Bit 7,6 - FIFOs Enabled (FEN1,0)

0 - No FIFO enabled. (Default)

1 - FIFOs are enabled (bit 0 of FCR is set to 1).

TABLE 7-3. Non-Extended Mode Interrupt Priorities

EIR Bits 3 2 1 0	Interrupt Set and Reset Functions			
	Priority Level	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0 0 0 1	-	None	None	-
0 1 1 0	Highest	Link Status	Parity error, framing error, data overrun or break event	Read Link Status Register (LSR).
0 1 0 0	Second	Receiver High Data Level Event	Receiver Holding Register (RXD) full, or RX_FIFO level equal to or above threshold.	Reading the RXD or, RX_FIFO level drops below threshold.
1 1 0 0	Second	RX_FIFO Time-Out	At least one character is in the RX_FIFO, and no character has been input to or read from the RX_FIFO for 4 character times.	Reading the RXD port.
0 0 1 0	Third	Transmitter Low Data Level Event	Transmitter Holding Register or TX_FIFO empty.	Reading the EIR Register if this interrupt is currently the highest priority pending interrupt, or writing into the TXD port.
0 0 0 0	Fourth	Modem Status	Any transition on $\overline{CTS}$, $\overline{DSR}$ or $\overline{DCD}$ or a low to high transition on $\overline{RI}$.	Reading the Modem Status Register (MSR).

Event Identification Register (EIR), Extended Mode

In Extended mode, each of the previously prioritized and encoded interrupt sources is broken down into individual bits. Each bit in this register acts as an interrupt pending flag, and is set to 1 when the corresponding event occurred or is pending, regardless of the IER register bit setting.

When this register is read the DMA event bit (bit 4) is cleared if an 8237 type DMA is used. All other bits are cleared when the corresponding interrupts are acknowledged by reading the relevant register (e.g. reading MSR clears MS_EV bit).

.

Extended Mode, Read Cycles

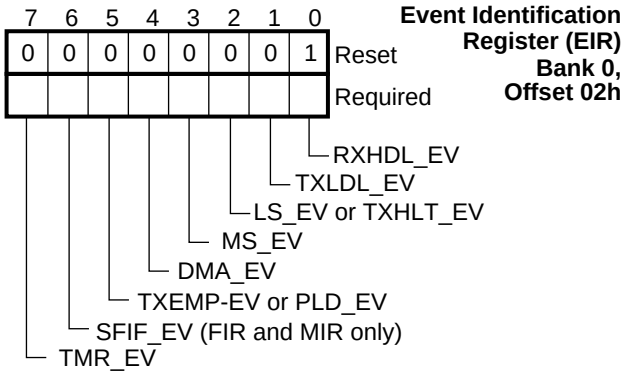


FIGURE 7-11. EIR Register Bitmap, Extended Mode

Bit 0 - Receiver High-Data-Level Event (RXHDL_EV)

When FIFOs are disabled, this bit is set to 1 when a character is in the Receiver Holding Register.

When FIFOs are enabled, this bit is set to 1 when the RX_FIFO is above threshold or an RX_FIFO time-out has occurred.

Bit 1 - Transmitter Low-Data-Level Event (TXLDL_EV)

When FIFOs are disabled, this bit is set to 1 when the Transmitter Holding Register is empty.

When FIFOs are enabled, this bit is set to 1 when the TX_FIFO is below the threshold level.

Bit 2 - Link Status Event (LS_EV) or Transmitter Halted Event (TXHLT_EV)

In the **UART, Sharp-IR** and **SIR** modes, this bit is set to 1 when a receiver error or break condition is reported.

When FIFOs are enabled, the Parity Error(PE), Frame Error(FE) and Break(BRK) conditions are only reported when the associated character reaches the bottom of the RX_FIFO. An Overrun Error (OE) is reported as soon as it occurs.

In the **MIR** and **FIR** modes, this bit indicates that a Link Status Event (LS_EV) or a Transmitter Halted Event (TXHLT_EV) occurred. It is set to 1 when any of the following conditions occurs:

— Last byte of receiver frame reaches the bottom of the RX_FIFO.

— A receiver overrun.

— A transmitter underrun .

— Transmitter halted on frame end.

In the **Consumer-IR** mode, this bit indicates that a Link Status Event (LS_EV) or a Transmitter Halted Event (TXHLT_EV) occurred. It is set to 1 when any of the following conditions occurs:

— A receiver overrun.

— A transmitter underrun .

Note: A high speed CPU can service the interrupt generated by the last frame byte reaching the RX_FIFO bottom before that byte is transferred to memory by the DMA controller. This can happen when the CPU interrupt latency is shorter than the FIFO Time-out event B (see sec. 7.9.2 on page 114). A DMA request is generated only when the RX_FIFO level reaches the DMA threshold or when Timeout Event B occurs, in order to minimize the performance degradation due to DMA signal handshake sequences.

If the DMA controller must be set up before receiving each frame, the software in the interrupt routine should make sure that the last byte of the frame just received has been transferred to memory before re-initializing the DMA controller, otherwise that byte could appear as the first byte of the next received frame.

Bit 3 - Modem Status Event (MS_EV)

In UART mode this bit is set to 1 when any of the 0 to 3 bits in the MSR register is set to 1.

In any **IR** mode, the function of this bit depends on the setting of the IRMSSL bit in the IRCR2 register (see Table 7-4 and also "Bit 1 - MSR Register Function Select in Infrared Mode (IRMSSL)" on page 138).

TABLE 7-4. Modem Status Event Detection Enable

IRMSSL Value	Bit Function
0	Modem Status Event (MS_EV)
1	Forced to 0.

Bit 4 - DMA Event Occurred (DMA_EV)

When an 8237 type DMA controller is used, this bit is set to 1 when a DMA terminal count (TC) is signalled. It is cleared upon read.

Bit 5 - Transmitter Empty (TXEMP_EV) or Pipeline Load Event (PLD_EV)

In **UART, Sharp-IR** and **Consumer-IR** modes, this bit is the same as bit 6 of the LSR register. It is set to 1 when the transmitter is empty.

In the **MIR, FIR** and **SIR** modes, this bit is set to 1 when the transmitter is empty or a pipeline operation occurs.

Bit 6 - ST_FIFO Event (SFIF_EV)

In **MIR** and **FIR** modes, this bit is set to 1 when the ST_FIFO level is equal to or above the threshold, or a ST_FIFO time-out occurs. This bit is cleared when the CPU reads the ST_FIFO and its level drops below the threshold.

Bit 7 - Timer Event (TMR_EV)

Set to 1 when the timer reaches 0.

Cleared by writing 1 into bit 7 of the ASCR register.

7.13.4 FIFO Control Register (FCR), Bank 0, Offset 02h

The FIFO Control Register (FCR) is write only. It is used to enable the FIFOs, clear the FIFOs and set the interrupt thresholds levels for the reception and transmission FIFOs.

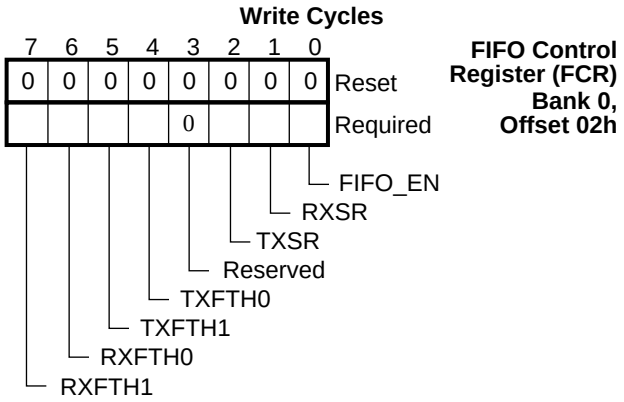


FIGURE 7-12. FCR Register Bitmap

Bit 0 - FIFO Enable (FIFO_EN)

When set to 1 enables both the Transmision and Reception FIFOs. Resetting this bit clears both FIFOs.

In **MIR**, **FIR** and **Consumer-IR** modes the FIFOs are always enabled and the setting of this bit is ignored.

Bit 1 - Receiver Soft Reset (RXSR)

Writing a 1 to this bit generates a receiver soft reset, which clears the RX_FIFO and the receiver logic. This bit is automatically cleared by the hardware.

Bit 2 - Transmitter Soft Reset (TXSR)

Writing a 1 to this bit generates a transmitter soft reset, which clears the TX_FIFO and the transmitter logic. This bit is automatically cleared by the hardware.

Bit 3 - Reserved

Read/Write 0.

Writing to this bit has no effect on the UART operation.

Bits 5,4 - TX_FIFO Threshold Level (TXFTH1,0)

In **Non-Extended** modes, these bits have no effect.

In **Extended** modes, these bits select the TX_FIFO interrupt threshold level. An interrupt is generated when the level of the data in the TX_FIFO drops below the encoded threshold.

TABLE 7-5. TX_FIFO Level Selection

TXFTH (Bits 5,4)	TX_FIF0 Tresh. (16 Levels)	TX_FIF0 Tresh. (32 Levels)
00(Default)	1	1
01	3	7
10	9	17
11	13	25

Bits 7,6 - RX_FIFO Threshold Level (RXFTH1,0)

In **Non-Extended** modes, these bits have no effect.

In **Extended** modes, these bits select the RX_FIFO interrupt threshold level. An interrupt is generated when the level of the data in the RX_FIFO is equal to or above the encoded threshold.

TABLE 7-6. RX_FIFO Level Selection

RXFTH (Bits 5,4)	RX_FIF0 Tresh. (16 Levels)	RX_FIF0 Tresh. (32 Levels)
00(Default)	1	1
01	4	8
10	8	16
11	14	26

7.13.5 Link Control Register (LCR), Bank 0, Offset 03h, and Bank Selection Register (BSR), All Banks, Offset 03h

The **Link Control Register (LCR)** and the **Bank Select Register (BSR)** (see the next register) share the same address.

The **Link Control Register (LCR)** selects the communications format for data transfers in UART, SIR and Sharp-IR modes.

Upon reset, all bits are set to 0.

Reading the register at this address location returns the content of the BSR. The content of LCR may be read from the Shadow of Link Control Register (SH_LCR) register in bank 3 (See Section 7.16.2 on page 134). During a write operation to this register at this address location, the setting of bit 7 (Bank Select Enable, BKSE) determines whether LCR or BSR is to be accessed, as follows:

- If bit 7 is 0, the write affects both LCR and BSR.
- If bit 7 is 1, and it is not one of the codes that selects bank 1 (see Table 7-9, "Bank Selection Encoding" on page 123), the write affects only BSR, and LCR remains unchanged. This prevents the communications format from being spuriously affected when a bank other than 0 or 1 is accessed.

Upon reset, all bits are set to 0.

Link Control Register (LCR), All Banks, Offset 03h

Bits 6-0 are only effective in **UART, Sharp-IR** and **SIR** modes. They are ignored in **MIR, FIR** and **Consumer-IR** modes

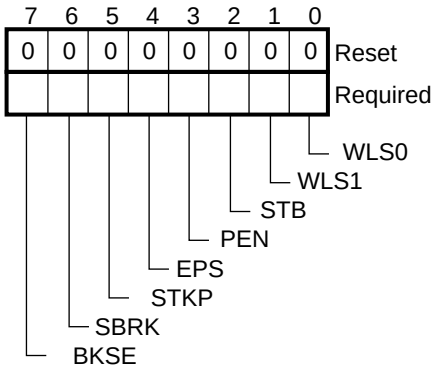


FIGURE 7-13. LCR Register Bitmap

Bits 1,0 - Character Length Select (WLS1,0)

These bits specify the number of data bits in each transmitted or received serial character. Table 7-7 shows how to encode these bits.

TABLE 7-7. Word Length Select Encoding

WLS1	WLS0	Character Length
0	0	5 (Default)
0	1	6
1	0	7
1	1	8

Bits 2 - Number of Stop Bits (STB)

This bit specifies the number of stop bits transmitted with each serial character.

0 - One stop bit is generated. (Default)

1 - If the data length is set to 5-bits via bits 1,0 (WLS1,0), 1.5 stop bits are generated. For 6, 7 or 8 bit word lengths, two stop bits are transmitted. The receiver checks for one stop bit only, regardless of the number of stop bits selected.

Bit 3 - Parity Enable (PEN)

This bit enable the parity bit See Table 7-8 on page 122.

The parity enable bit is used to produce an even or odd number of 1s when the data bits and parity bit are summed, as an error detection device.

0 - No parity bit is used. (Default)

1 - A parity bit is generated by the transmitter and checked by the receiver.

Bit 4 - Even Parity Select (EPS)

When Parity is enabled (PEN is 1), this bit, together with bit 5 (STKP), controls the parity bit as shown in Table 7-8.

0 - If parity is enabled, an odd number of logic 1s are transmitted or checked in the data word bits and parity bit. (Default)

1 - If parity is enabled, an even number of logic 1s are transmitted or checked.

Bit 5 - Stick Parity (STKP)

When Parity is enabled (PEN is 1), this bit, together with bit 4 (EPS), controls the parity bit as show in Table 7-8.

TABLE 7-8. Bit Settings for Parity Control

PEN	EPS	STKP	Selected Parity Bit
0	x	x	None
1	0	0	Odd
1	1	0	Even
1	0	1	Logic 1
1	1	1	Logic 0

Bit 6 - Set Break (SBRK)

This bit enables or disables a break. During the break, the transmitter can be used as a character timer to accurately establish the break duration.

This bit acts only on the transmitter front-end and has no effect on the rest of the transmitter logic.

When set to 1 the following occurs:

— If a **UART** mode is selected, the SOUT pin is forced to a logic 0 state.

— If **SIR** mode is selected, pulses are issued continuously on the IRTX pin.

— If **Sharp-IR** mode is selected and internal modulation is enabled, pulses are issued continuously on the IRTX pin.

— If **Sharp-IR** mode is selected and internal modulation is disabled, the IRTX pin is forced to a logic 1 state.

To avoid transmission of erroneous characters as a result of the break, use the following procedure to set SBRK:

1. Wait for the transmitter to be empty. (TXEMP = 1).
2. Set SBRK to 1.
3. Wait for the transmitter to be empty, and clear SBRK when normal transmission must be restored.

Bit 7 - Bank Select Enable (BKSE)

0 - This register functions as the Link Control Register (LCR).

1 - This register functions as the Bank Select Register (BSR).

7.13.6 Bank Selection Register (BSR), All Banks, Offset 03h

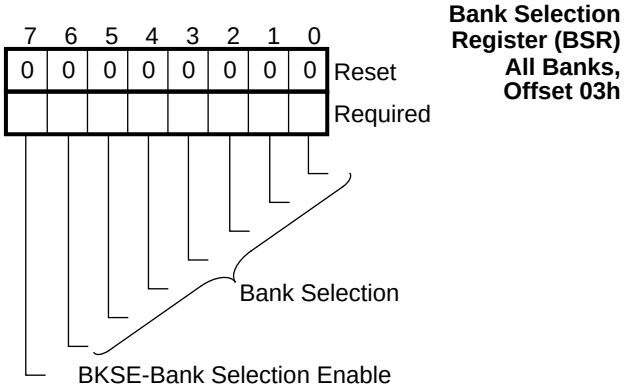


FIGURE 7-14. BSR Register Bitmap

The Bank Selection Register (BSR) selects which register bank is to be accessed next.

About accessing this register see the description of bit 7 of the LCR Register.

Bits 6-0 - Bank Selection

When bit 7 is set to 1, bits 6-0 of BSR select the bank, as shown in Table 7-9.

Bit 7 - Bank Selection Enable (BKSE)

0 - Bank 0 is selected.

1 - Bits 6-0 specify the selected bank.

TABLE 7-9. Bank Selection Encoding

BSR Bits								Bank Selected	LCR
7	6	5	4	3	2	1	0		
0	x	x	x	x	x	x	x	0	LCR is written
1	0	x	x	x	x	x	x	1	
1	1	x	x	x	x	1	x	1	
1	1	x	x	x	x	x	1	1	
1	1	1	0	0	0	0	0	2	LCR is not written
1	1	1	0	0	1	0	0	3	
1	1	1	0	1	0	0	0	4	
1	1	1	0	1	1	0	0	5	
1	1	1	1	0	0	0	0	6	
1	1	1	1	0	1	0	0	7	
1	1	1	1	1	x	0	0	Reserved	
1	1	0	x	x	x	0	0	Reserved	

7.13.7 Modem/Mode Control Register (MCR), Bank 0, Offset 04h

This register controls the interface with the modem or data communications set, and the device operational mode when the device is in the **Extended** mode. The register function differs for Extended and Non-Extended modes.

Modem/Mode Control Register (MCR), Non-Extended Mode, Bank 0, Offset 04h

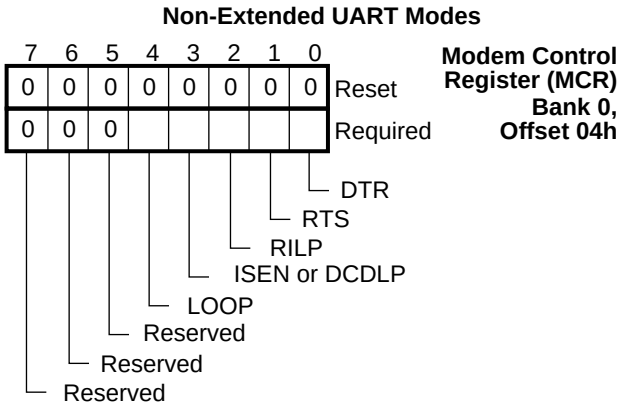


FIGURE 7-15. MCR Register Bitmap, Non-Extended Mode

Bit 0 - Data Terminal Ready (DTR)

This bit controls the $\overline{DTR}$ signal output. When set to 1, $\overline{DTR}$ is driven low. When loopback is enabled (LOOP is set to 1), this bit internally drives $\overline{DSR}$.

Bit 1 - Request To Send (RTS)

This bit controls the $\overline{RTS}$ signal output. When set to 1, drives $\overline{RTS}$ low. When loopback is enabled (LOOP is set), this bit drives $\overline{CTS}$, internally.

Bit 2 - Loopback Interrupt Request (RILP)

When loopback is enabled, this bit internally drives $\overline{RI}$. Otherwise it is unused.

Bit 3 - Interrupt Signal Enable (ISEN) or Loopback DCD (DCDLP)

In normal operation (standard 16450 or 16550) mode, this bit controls the interrupt signal and must be set to 1 in order to enable the interrupt request signal.

When loopback is enabled, the interrupt output signal is always enabled, and this bit internally drives $\overline{DCD}$.

New programs should always keep this bit set to 1 during normal operation. The interrupt signal should be controlled through the Plug-n-Play logic.

Bit 4 - Loopback Enable (LOOP)

When this bit is set to 1, it enables loopback. This bit accesses the same internal register as bit 4 of the EXCR1 register. (see ”Extended Control Register 1 (EXCR1), Bank 2, Offset 02h” on page 130 for more information on the Loopback mode).

0 - Loopback disabled. (Default)

1 - Loopback enabled.

Bits 7-5 - Reserved

Read/Write 0.

Modem/Mode Control Register (MCR), Extended Mode, Bank 0, Offset 04h

In Extended mode, this register is used to select the operation mode (IrDA, Sharp, etc.) of the device and to enable the DMA interface. In these modes, the interrupt output signal is always enabled, and loopback can be enabled by setting bit 4 of the EXCR1 register.

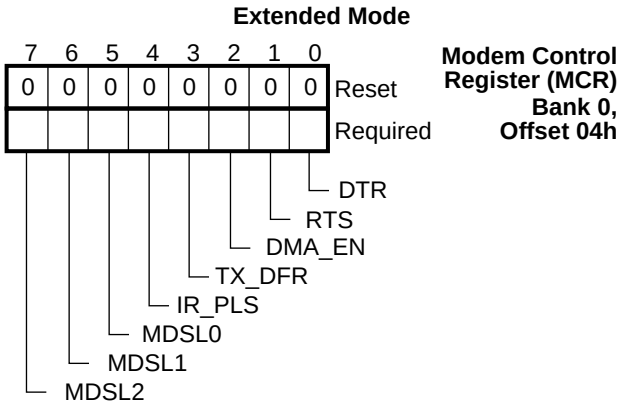


FIGURE 7-16. MCR Register Bitmap, Extended Modes

Bit 0 - Data Terminal Ready (DTR)

This bit controls the $\overline{DTR}$ signal output. When set to1, $\overline{DTR}$ is driven low. When loopback is enabled (LOOP is set), this bit internally drives both $\overline{DSR}$ and $\overline{RI}$.

Bit 1 - Request To Send (RTS)

This bit controls the $\overline{RTS}$ signal output. When set to1, $\overline{RTS}$ is driven low. When loopback is enabled (LOOP is set), this bit internally drives both $\overline{CTS}$ and $\overline{DCD}$.

Bit 2 - DMA Enable (DMA_EN)

When set to1, DMA mode of operation is enabled. When DMA is selected, transmit and/or receive interrupts should be disabled to avoid spurious interrupts.

DMA cycles always address the Data Holding Registers or FIFOs, regardless of the selected bank.

Bit 3 - Transmission Deferral (TX_DFR)

For a detailed description of the Transmission Deferral see ”Transmission Deferral” on page 114.

0 - No transmission deferral enabled. (Default)

1 - Transmission deferral enabled.

This bit is effective only if the Transmission FIFOs is enabled.

Bit 4 - Send Interaction Pulse (IR_PLS)

This bit is effective only in **MIR** or **FIR** modes.

When set to 1, a 2µsec infrared interaction pulse is transmitted at the end of the frame and it is automatically cleared after the pulse is sent. This 2 µsec pulse indicates to low speed devices that high speed transfers are taking place.

This bit is automatically cleared after the pulse is sent or if the mode changes or after “soft reset”.

Writing 0 into it has no effect.

Bits 7-5 - Mode Select (MDSL2-0)

These bits select the operational mode of the module when in **Extended** mode, as shown in Table 7-10.

When the mode is changed, the transmission and reception FIFOs are flushed, Link Status and Modem Status Interrupts are cleared, and all of the bits in the auxiliary status and control register are cleared.

TABLE 7-10. The Module Operation Modes

MDSL2 (Bit 7)	MDSL1 (Bit 6)	MDSL0 (Bit 5)	Operational Mode
0	0	0	UART Modes (Default)
0	0	1	Reserved
0	1	0	Sharp-IR
0	1	1	SIR
1	0	0	MIR
1	0	1	FIR
1	1	0	Consumer-IR
1	1	1	Reserved

7.13.8 Link Status Register (LSR), Bank 0, Offset 05h

This register provides status information concerning the data transfer. The bits indicating the error conditions are sticky (they accumulate the occurrence of error conditions since the last time they were read). They are cleared when one of the following events occurs:

- A hardware reset occurs.
- The receiver is soft-reset.
- The LSR register is read.

Upon reset this register assumes the value of 0x60h.

The bit definitions change depending upon the operation mode of the module.

Bits 4 through 1 of the LSR are the error conditions that generate a Receiver Link Status interrupt whenever any of the corresponding conditions are detected and that interrupt is enabled.

The LSR is intended for read operations only. Writing to the LSR is not permitted

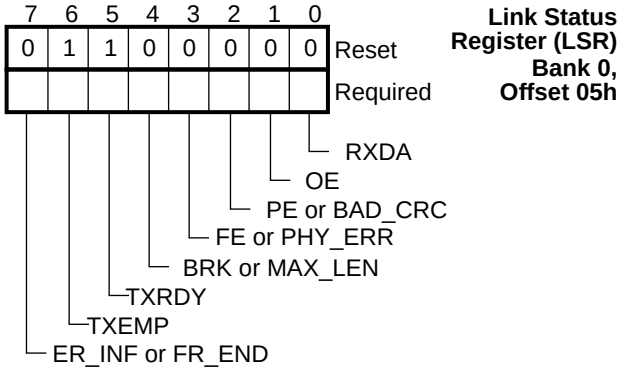


FIGURE 7-17. LSR Register Bitmap

Bit 0 - Receiver Data Available (RXDA)

Set to 1 when the Receiver Holding Register is full.

If the FIFOs are enabled, this bit is set when at least one character is in the RX_FIFO.

Cleared when the CPU reads all the data in the Holding Register or in the RX_FIFO.

Bit 1 - Overrun Error (OE)

This bit is set to 1 as soon as an overrun condition is detected by the receiver.

Cleared upon read.

In **UART, Sharp-IR, SIR** and **Consumer-IR** modes when-

FIFOs Disabled:

An overrun occurs when a new character is completely received into the receiver front-end section and the CPU has not yet read the previous character in the receiver holding register. The new character is discarded, and the receiver holding register is not affected.

FIFOs Enabled:

An overrun occurs when a new character is completely received into the receiver front-end section and the RX_FIFO is full. The new character is discarded, and the RX_FIFO is not affected.

In the **MIR** and **FIR** modes, an overrun occurs when a new character is completely received into the receiver front-end section and the RX_FIFO or the ST_FIFO is full. The new character is discarded, and the RX_FIFO is not affected.

Bit 2 - Parity Error or CRC Error (PE or BAD_CRC)

In **UART, Sharp-IR** and **SIR** modes, this bit is set to 1 if the received data character does not have the correct parity, even or odd as selected by the parity control bits of the LCR register.

If the FIFOs are enabled, this error is associated with the particular character in the FIFO that it applies to. This error is revealed to the CPU when its associated character is at the bottom of the RX_FIFO.

In **MIR** and **FIR** modes, this bit is the **BAD_CRC** bit. It set to 1 when the received CRC and the receiver-generated CRC do not match, and the last byte has reached the bottom of the RX_FIFO.

This bit is cleared upon read.

Bit 3 - Framing Error or Physical Layer Error (FE or PHY_ERR)

In **UART, Sharp-IR** and **SIR** modes, this bit is set to 1 when the received data character does not have a valid stop bit (i.e., the stop bit following the last data bit or parity bit is a 0).

If the FIFOs are enabled, this Framing Error is associated with the particular character in the FIFO that it applies to. This error is revealed to the CPU when its associated character is at the bottom of the RX_FIFO.

After a framing error is detected, the receiver will try to resynchronize.

If the bit following the erroneous stop bit is 0, the receiver assumes it to be a valid start bit and shifts in the new character. If that bit is a 1, the receiver enters the idle state and awaits the next start bit.

In **MIR** mode this bit is the **PHY_ERR** (Physical Layer Error) bit. It is set to 1 when an abort condition is detected during the reception of a frame, and the last byte of the frame has reached the bottom of the RX_FIFO.

In **FIR** mode this bit is the **PHY_ERR** (Physical Layer Error) bit. It is set to 1 when an encoding error or the sequence BOF-data-BOF is detected (missing EOF) during the reception of a frame, and the last byte of the frame has reached the bottom of the RX_FIFO.

This bit is cleared upon read.

Bit 4 - Break Event Detected or Maximum Length Exceeded (BRK or MAX_LEN)

In **UART, Sharp-IR** and **SIR** modes this bit is set to 1 when a break event is detected (i.e. when a sequence of logic 0 bits, equal or longer than a full character transmission, is received). If the FIFOs are enabled, the break condition is associated with the particular character in the RX_FIFO to which it applies. In this case, the BRK bit is set when the character reaches the bottom of the RX_FIFO.

When a break event occurs, only one zero character is transferred to the Receiver Holding Register or to the RX_FIFO.

The next character transfer takes place after at least one logic 1 bit is received followed by a valid start bit.

In **MIR** and **FIR** modes, this is the **MAX_LEN** (Maximum Length exceeded) bit. It is set to 1 when a frame exceeding the maximum length has been received, and the last byte of the frame has reached the bottom of the RX_FIFO.

This bit is cleared upon read.

Bit 5 - Transmitter Ready (TXRDY)

This bit is set to 1 when the Transmitter Holding Register or the TX_FIFO is empty.

It is cleared when a data character is written to the TXD register.

Bit 6 - Transmitter Empty (TXEMP)

This bit is set to 1 when the Transmitter Holding Register or the TX_FIFO is empty, and the transmitter front-end is idle.

Bit 7 - Error in RX_FIFO (ER_INF) or Frame End (FR_END)

In **UART, Sharp-IR** and **SIR** modes, this bit is set to a 1 if there is at least 1 framing error, parity error or break indication in the RX_FIFO.

This bit is always 0 in the 16450 mode.

In the **MIR** and **FIR** modes, this is the Frame End (FR_END) bit. It is set to 1 when the last byte of a received frame reaches the bottom of the RX_FIFO.

This bit is cleared upon read.

7.13.9 Modem Status Register (MSR), Bank 0, Offset 06h

The function of this register depends on the selected operational mode. When a **UART** mode is selected, this register provides the current-state as well as state-change information of the status lines from the modem or data transmission module.

When any of the infrared modes is selected, the register function is controlled by the setting of the **IRMSSL** bit in the IRCR2 (see page 138). If IRMSSL is 0, the MSR register works as in UART mode. If IRMSSL is 1, the MSR register returns the value 30 hex, regardless of the state of the modem input lines.

When loopback is enabled, the MSR register works similarly except that its status input signals are internally driven by appropriate bits in the MCR register since the modem input lines are internally disconnected. Refer to the DTR & RTS bits at the MCR (see page 123) and to the LOOP & ETDLBK bits at the EXCR1 (see page 130) for more information.

A description of the various bits of the MSR register, with Loopback disabled and UART Mode selected, is provided below.

When bits 0, 1, 2 or 3 is set to 1, a Modem Status Event (MS_EV) is generated if the MS_IE bit is enabled in the IER

Bits 0 to 3 are set to 0 as a result of any of the following events:

- A hardware reset occurs.
- The operational mode is changed and the IRMSSL bit is 0.
- The MSR register is read.

In the reset state, bits 4 through 7 are indeterminate as they reflect their corresponding input signals.

Note: The modem status lines can be used as general purpose inputs. They have no effect on the transmitter or receiver operation.

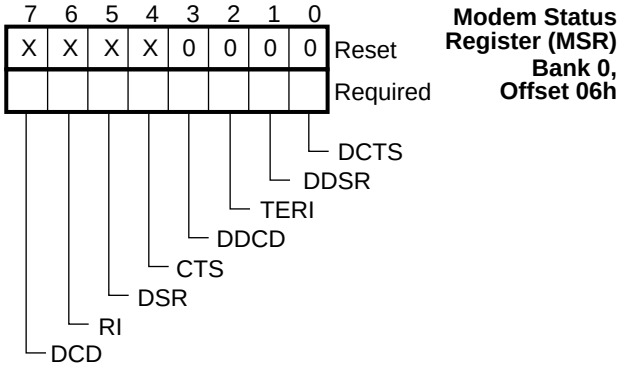


FIGURE 7-18. MSR Register Bitmap

Bit 0 - Delta Clear to Send (DCTS)

Set to 1, when the $\overline{CTS}$ input signal changes state.

This bit is cleared upon read.

Bit 1 - Delta Data Set Ready (DDSR)

Set to 1, when the $\overline{DSR}$ input signal changes state.

This bit is cleared upon read

Bit 2 - Trailing Edge Ring Indicate (TERI)

Set to 1, when the $\overline{RI}$ input signal changes state from low to high.

This bit is cleared upon read

Bit 3 - Delta Data Carrier Detect (DDCD)

Set to 1, when the $\overline{DCD}$ input signal changes state.

1 - $\overline{DCD}$ signal state changed.

Bit 4 - Clear To Send (CTS)

This bit returns the inverse of the $\overline{CTS}$ input signal.

Bit 5 - Data Set Ready (DSR)

This bit returns the inverse of the $\overline{DSR}$ input signal.

Bit 6 - Ring Indicate (RI)

This bit returns the inverse of the $\overline{RI}$ input signal.

Bit 7 - Data Carrier Detect (DCD)

This bit returns the inverse of the $\overline{DCD}$ input signal.

7.13.10 Scratchpad Register (SPR), Bank 0, Offset 07h

This register shares a common address with the following one (ASCR).

In the **Non-Extended** mode this is a scratch register (as in the 16550) for temporary data storage.

Non-Extended Modes

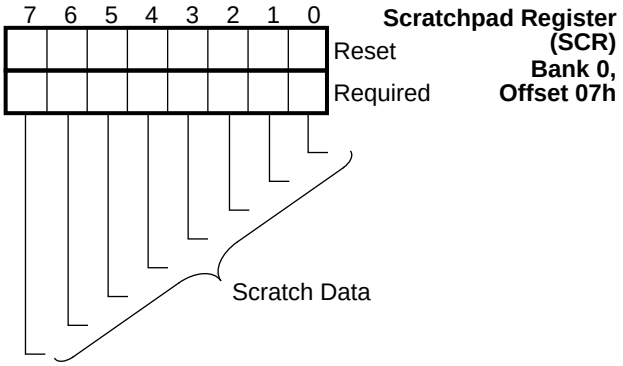


FIGURE 7-19. SPR Register Bitmap

7.13.11 Auxiliary Status and Control Register (ASCR), Bank 0, Offset 07h

This register shares a common address with the previous one (SCR).

This register is accessed when the **Extended** mode of operation is selected. The definition of the bits in this case is dependent upon the mode selected in the MCR register, bits 7 through 5. This register is cleared upon hardware reset or when the operational mode changes. Bits 2 and 6 are cleared when the transmitter is “soft reset”. Bits 0,1,4 and 5 are cleared when the receiver is “soft reset”.

Extended Modes

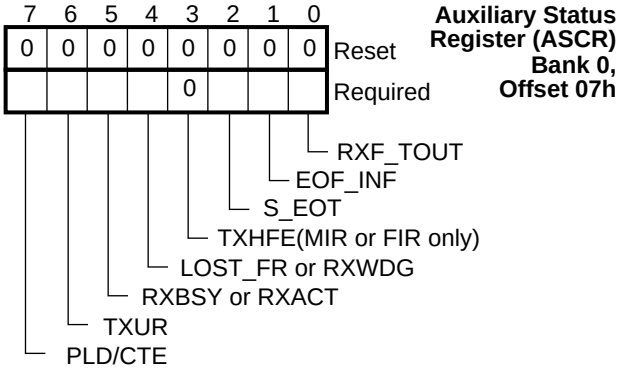


FIGURE 7-20. ASCR Register Bitmap

Bit 0 - RX_FIFO Time-Out (RXF_TOUT)

This bit is read only and set to 1 when an RX_FIFO timeout occurs. It is cleared when a character is read from the RX_FIFO.

Note: In **MIR** or **FIR** mode, this bit can be used in conjunction with bit 1 (EOT_INF) to determine whether a number of bytes (as determined by the RX_FIFO threshold), can be read without checking the RXDA bit in the LSR register for each byte.

Bit 1 - Frame End In FIFO (EOF_INF)

In **MIR** or **FIR** mode, this bit is read only and set to 1 when one or more EOF bytes are in the RX_FIFO. It is cleared when no EOF byte is in the RX_FIFO.

Bit 2 - Set End of Transmission (S_EOT)

In **MIR** or **FIR** modes, this is the Set End of Transmission bit. When a 1 is written into this bit position before writing the last character into the TX_FIFO, frame transmission is completed and a CRC + EOF is sent.

This bit can be used as an alternative to the TFRL/TFRCC counter (see page 135). If this method is to be used, the FEND_MD bit in the IRCR2 (see page 138) should be set to 1 or the Transmission Frame Length Register should be set to maximum count. This bit is automatically cleared by hardware when a character is written to the TX_FIFO.

In **Consumer-IR** mode this is the Set End of Transmission bit. When a 1 is written into this bit position before writing the last character into the TX_FIFO, data transmission is gracefully completed.

In this mode, if the CPU simply stops writing data into the TX_FIFO at the end of the data stream, a transmitter underrun is generated and the transmitter stops. In this case this is not an error, but the software must clear the underrun before the next transmission can occur. This bit is automatically cleared by hardware when a character is written to the TX_FIFO.

Bit 3 - Transmitter Halted on Frame End (TXHFE)

This bit is used only in **MIR** or **FIR** modes, when the Transmitter Frame End Stop mode is selected (TX_MS bit in IRCR2 (see page 138) is set to 1). It is set to 1 by the hardware when transmission of a frame is completed and an End Of Frame condition is generated by the TRFCC (see page 135) counter reaches 0.

This bit must be cleared, by writing 1 into it, to re-enable transmission.

Bit 4 - Lost Frame Flag (LOST_FR) or Reception Watchdog (RXWDG)

In the **MIR** or **FIR** modes, this is the Lost Frame Flag. This read-only bit reflects the setting of the lost-frame indicator flag at the bottom of the ST_FIFO.

In **Consumer-IR** mode, this is the Reception Watchdog (RXWDG) bit. It is set to 1 each time a pulse or pulse-train (modulated pulse) is detected by the receiver. It can be used by the software to detect a receiver idle condition. It is cleared upon read.

Bit 5 - Receiver Busy (RXBSY) or Receiver Active (RXACT)

In the **MIR** or **FIR** modes, this is the Receiver Busy (RXBSY) bit. It is a read only bit and is set to 1 when reception of a frame is in progress.

In **Consumer-IR** Mode this is the Receiver Active (RXACT) bit. It is set to 1 when an infrared pulse or pulse-train is received. If a 1 is written into this bit position, the bit is cleared and the receiver is deactivated. When this bit is set, the receiver samples the infrared input continuously at the programmed baud rate and transfers the data to the RX_FIFO. See ”Consumer-IR Reception” on page 113.

Bit 6 - Infrared Transmitter Underrun (TXUR)

In the **MIR**, **FIR** and **Consumer-IR** modes, this is the Transmitter Underrun flag. This bit is set to 1 when a transmitter underrun occurs. It is always cleared when a mode other than MIR, FIR or Consumer-IR is selected. This bit must be cleared, by writing 1 into it, to re-enable transmission.

Bit 7 - Pipeline Status (PLD) or Clear Timer Event (CTE)

In **MIR, FIR** or **SIR** modes, on a read operation, this is the Pipeline Load Status (PLD) bit. Reading this bit returns the pipeline load status. This bit is set to 1 when a pipeline load operation occurs, and is cleared upon read.

In all the other Extended Modes, writing 1 into this bit position clears the TMR_EV bit in the EIR register. Writing 0 into this bit has no effect.

The write operation has no effect on the Pipeline Load Status bit.

7.14 BANK 1 – THE LEGACY BAUD RATE GENERATOR DIVISOR PORTS

This register bank contains two baud rate generator divisor ports, and a bank select register.

The Legacy Baud-rate Generator Divisor (LBGD) port provides an alternate path to the Baud Divisor Generator register. This bank is implemented to maintain compatibility with 16550 standard and to support existing legacy software packages. In case of using legacy software, the addresses 0 and 1 are shared with the data ports RXD/TXD (see page 116). The selection between them is controlled by the value of the BKSE bit (LCR bit 7 page 122).

TABLE 7-11. Bank 1 Register Set

Offset	Register Name	Description
00h	LBGD(L)	Legacy Baud Rate Generator Divisor Port (Low Byte)
01h	LBGD(H)	Legacy Baud Rate Generator Divisor Port (High Byte)
02h	Reserved	
03h	LCR/ BSR	Link Control / Bank Select Register
04h - 07h	Reserved	

In addition, a fallback mechanism maintains this compatibility by forcing the UART to revert to 16550 mode if 16550 software addresses the module after a different mode was set. Since setting the baud rate divisor values is a necessary initialization of the 16550, setting the divisor values in bank 1 forces the UART to enter 16550 mode. (This is called fallback.)

To enable other modes to program their desired baud rates without activating this fallback mechanism, the baud rate divisor register in bank 2 should be used.

7.14.1 Legacy Baud Rate Generator Divisor Ports (LBGD(L) and LBGD(H)), Bank 1, Offsets 00h and 01h

The programmable baud rates in the Non-Extended mode are achieved by dividing a 24 MHz clock by a prescale value of 13, 1.625 or 1. This prescale value is selected by the PRESL field of EXCR2 (see page 132). This clock is subdivided by the two baud rate generator divisor buffers, which output a clock at 16 times the desired baud rate (this clock is the BAUDOUT clock). This clock is used by I/O circuitry, and after a last division by 16 produces the output baud rate.

Divisor values between 1 and 2^{16}-1 can be used. (Zero is forbidden). The baud rate generator divisor must be loaded during initialization to ensure proper operation of the baud rate generator. Upon loading either part of it, the baud rate generator counter is immediately loaded. Table 7-15 on page 131 shows typical baud rate divisors.After reset the divisor register contents are indeterminate.

Any access to the **LBGD(L)** or **LBGD(H)** ports causes a reset to the default Non-Extended mode, i.e., 16550 mode (See "Automatic Fallback to A Non-Extended UART Mode" on page 115).To access a Baud Rate Generator Divisor when in the **Extended** mode, use the port pair in bank 2 (BGD on page 129).

Table 7-12 shows the bits which are cleared when Fallback occurs during **Extended** or **Non-Extended** modes.If the UART is in **Non-Extended** mode and the LOCK bit is 1, the content of the divisor (BGD) ports will not be affected and no other action is taken.

When programming the baud rate, the new divisor is loaded upon writing into LBGD(L) and LBGD(H). After reset, the contents of these registers are indeterminate.

Divisor values between 1 and 2^{16}-1 can be used. (Zero is forbidden.) Table 7-14 shows typical baud rate divisors.

TABLE 7-12. Bits Cleared On Fallback

Register	UART Mode & LOCK bit before Fallback		
	Extended Mode LOCK = x	Non-Extended Mode LOCK = 0	Non-Extended Mode LOCK = 1
MCR	2 to 7	none	none
EXCR1	0, 5 and 7	5 and 7	none
EXCR2	0 to 5	0 to 5	none
IRCR1	2 and 3	none	none

.

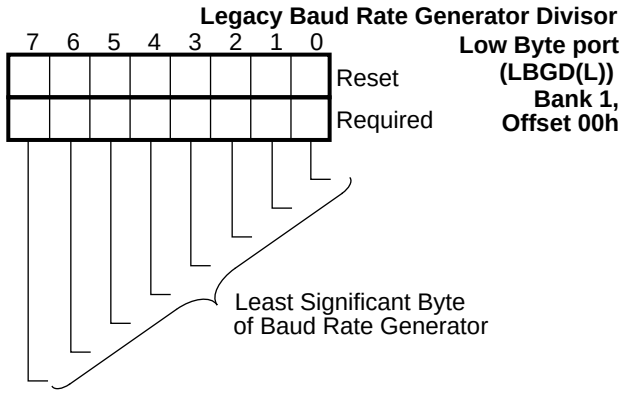


FIGURE 7-21. LBGD(L) Register Bitmap

.

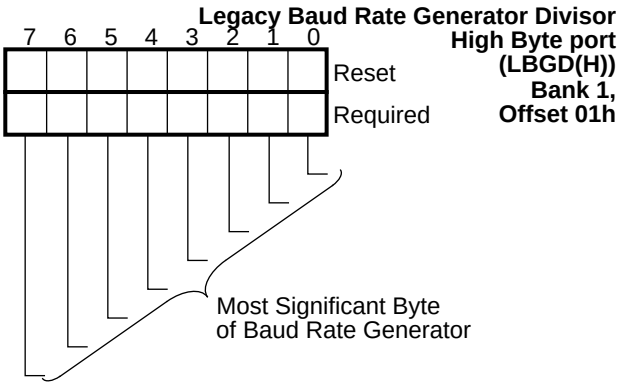


FIGURE 7-22. LBGD(H) Register Bitmap

7.14.2 Link Control Register (LCR) and Bank Select Register (BSR), Bank 1, Offset 03h

These registers are the same as the registers at offset 03h in bank 0.

7.15 BANK 2 – EXTENDED CONTROL AND STATUS REGISTERS

Bank 2 contains two alternate Baud rate Generator Divisor ports and the Extended Control Registers (EXCR1 and EXCR2).

TABLE 7-13. Bank 2 Register Set

Offset	Register Name	Description
00h	BGD(L)	Baud Rate Generator Divisor Port (Low byte)
01h	BGD(H)	Baud Rate Generator Divisor Port (High byte)
02h	EXCR1	Extended Control Register 1
03h	LCR/BSR	Link Control/ Bank Select Register
04h	EXCR2	Extended Control Register 2
05h	Reserved	
06h	TXFLV	TX_FIFO Level
07h	RXFLV	RX_FIFO Level

7.15.1 Baud Rate Generator Divisor Ports, LSB (BGD(L)) and MSB (BGD(H)), Bank 2, Offsets 00h and 01h

These ports perform the same function as the Legacy Baud Divisor Ports in Bank 1 and are accessed identically to them, but do not change the operation mode of the module when accessed. Refer to Section 7.14.1 on page 128 for more detail.

These ports should be used to set the baud rate when operating in Extended mode to avoid fallback to a Non-Extended operation mode, i.e., 16550 compatible.

When programming the baud rate, writing to BGDH causes the baud rate to change immediately.

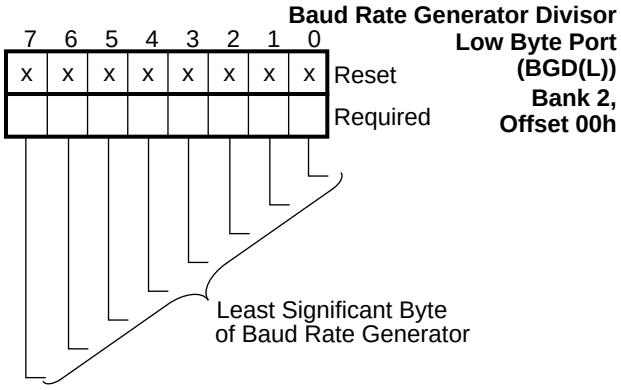


FIGURE 7-23. BGD(L) Register Bitmap

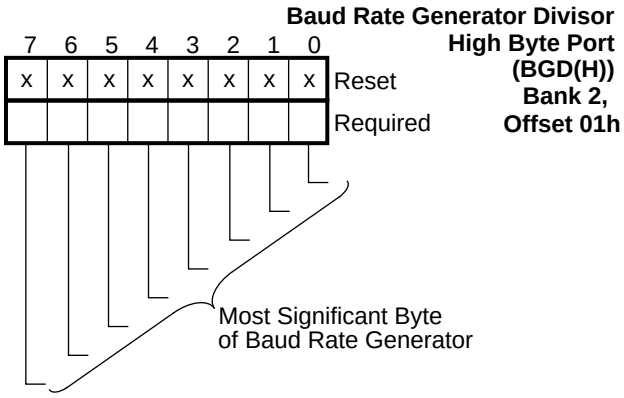


FIGURE 7-24. BGD(H) Register Bitmap

TABLE 7-14. Baud Rate Generator Divisor settings

Prescaler Value	13		1.625		1	
Baud Rate	**Divisor**	**% Error**	**Divisor**	**% Error**	**Divisor**	**% Error**
50	2304	0.16%	18461	0.00%	30000	0.00%
75	1536	0.16%	12307	0.01%	20000	0.00%
110	1047	0.19%	8391	0.01%	13636	0.00%
134.5	857	0.10%	6863	0.00%	11150	0.02%
150	768	0.16%	6153	0.01%	10000	0.00%
300	384	0.16%	3076	0.03%	5000	0.00%
600	192	0.16%	1538	0.03%	2500	0.00%
1200	96	0.16%	769	0.03%	1250	0.00%
1800	64	0.16%	512	0.16%	833	0.04%
2000	58	0.53%	461	0.12%	750	0.00%
2400	48	0.16%	384	0.16%	625	0.00%
3600	32	0.16%	256	0.16%	416	0.16%
4800	24	0.16%	192	0.16%	312	0.16%
7200	16	0.16%	128	0.16%	208	0.16%
9600	12	0.16%	96	0.16%	156	0.16%
14400	8	0.16%	64	0.16%	104	0.16%
19200	6	0.16%	48	0.16%	78	0.16%
28800	4	0.16%	32	0.16%	52	0.16%
38400	3	0.16%	24	0.16%	39	0.16%
57600	2	0.16%	16	0.16%	26	0.16%
115200	1	0.16%	8	0.16%	13	0.16%
230400	---	---	4	0.16%	---	---
460800	---	---	2	0.16%	---	---
750000	---	---	---	---	2	0.00%
921600	---	---	1	0.16%	---	---
1500000	---	---	---	---	1	0.00%

7.15.2 Extended Control Register 1 (EXCR1), Bank 2, Offset 02h

Use this register to control module operation in the Extended mode. Upon reset all bits are set to 0.

Extended Control and and Status Register 1 (EXCR1) Bank 2, Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
	1							Required

EXT_SL
DMANF
DMATH
DMASWP
LOOP
ETDLBK
Reserved
BTEST

EXCR1 Register BitmapBit 0 - Extended Mode Select (EXT_SL)

When set to 1, the Extended mode is selected.

Bit 1 - DMA Fairness Control (DMANF)

This bit controls the maximum duration of DMA burst transfers.

0 - DMA requests are forced inactive after approximately 10.5 µsec of continuous transmitter and/or receiver DMA operation. (Default)

1 - A transmission DMA request is deactivated when the TX_FIFO is full. A reception DMA request is deactivated when the RX_FIFO is empty.

Bit 2 - DMA FIFO Threshold (DMATH)

This bit selects the TX_FIFO and RX_FIFO threshold levels used by the DMA request logic to support demand transfer mode.

A transmission DMA request is generated when the TX_FIFO level is below the threshold.

A reception DMA request is generated when the RX_FIFO level reaches the threshold or when a DMA timeout occurs.

Table 7-15 lists the threshold levels for each FIFO.

TABLE 7-15. DMA Threshold Levels

Bit Value	DMA Threshold for FIFO Type		
	RX_FIFO	Tx_FIFO (16 Levels)	Tx_FIFO (32 Levels)
0	4	13	29
1	10	7	23

Bit 3 - DMA Swap (DMASWP)

This bit selects the routing of the DMA control signals between the internal DMA logic and the configuration module of the chip. When this bit is 0, the transmitter and receiver DMA control signals are not swapped. When it is 1, they are swapped. A block diagram illustrating the control signals routing is given in Fig. 7-25.

The swap feature is particularly useful when only one 8237 DMA channel is used to serve both transmitter and receiver. In this case only one external DRQ/DACK signal pair will be interconnected to the swap logic by the configuration module. Routing the external DMA channel to either the transmitter or the receiver DMA logic is then simply controlled by the DMASWP bit. This way, the infrared device drivers do not need to know the details of the configuration module.

.

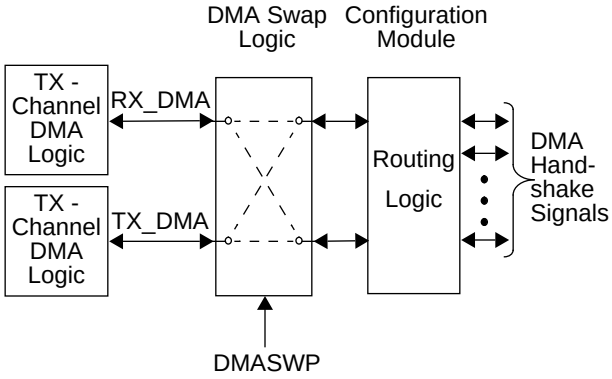


FIGURE 7-25. DMA Control Signals Routing

Bit 4 - Loopback Enable (LOOP)

During loopback, the transmitter output is connected internally to the receiver input, to enable system self-test of serial communications. In addition to the data signal, all additional signals within the UART are interconnected to enable real transmission and reception using the UART mechanisms.

When this bit is set to 1, loopback is selected. This bit accesses the same internal register as bit 4 in the MCR register, when the UART is in a Non-Extended mode.

Loopback behaves similarly in both Non-Extended and Extended modes.

When Extended mode is selected, the $\overline{DTR}$ bit in the MCR register internally drives both $\overline{DSR}$ and $\overline{RI}$, and the $\overline{RTS}$ bit drives $\overline{CTS}$ and $\overline{DCD}$.

During loopback, the following actions occur:

1. The transmitter and receiver interrupts are fully operational. The Modem Status Interrupts are also fully operational, but the interrupt sources are now the lower bits of the MCR register. Modem interrupts in infrared modes are disabled unless the IRMSSL bit in the IRCR2 register is 0. Individual interrupts are still controlled by the IER register bits.
2. The DMA control signals are fully operational.
3. UART and infrared receiver serial input signals are disconnected. The internal receiver input signals are connected to the corresponding internal transmitter output signals.
4. The UART transmitter serial output is forced high and the infrared transmitter serial output is forced low, unless the ETDLBK bit is set to 1. In which case they function normally.
5. The modem status input pins ($\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$ and $\overline{DCD}$) are disconnected. The internal modem status signals, are driven by the lower bits of the MCR register.

Bit 5 - Enable Transmitter During Loopback (ETDLBK)

When this bit is set to 1, the transmitter serial output is enabled and functions normally when loopback is enabled.

Bit 6 - Reserved

Write 1.

Bit 7 - Baud Rate Generator Test (BTEST)

When set, this bit routes the baud rate generator to the $\overline{DTR}$ pin for testing purposes.

7.15.3 Link Control Register (LCR) and Bank Select Register (BSR), Bank 2, Offset 03h

These registers are the same as the registers at offset 03h in bank 0.

7.15.4 Extended Control and Status Register 2 (EXCR2), Bank 2, Offset 04h

This register configures the transmitter and receiver FIFOs, and the baud rate generator prescaler.

Upon reset all bits are set to 0.

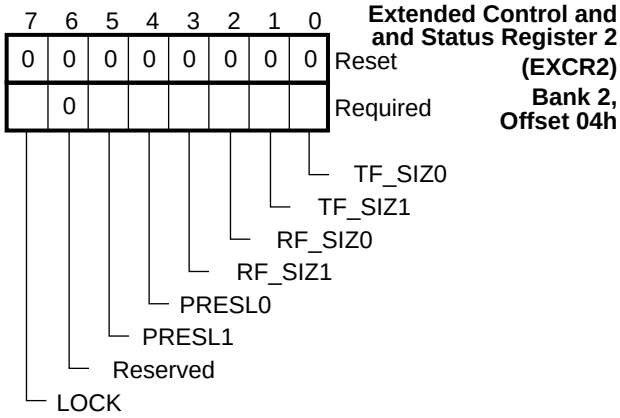


FIGURE 7-26. EXCR2 Register Bitmap

Bits 1,0 - TX_FIFO Size (TF_SIZ1,0)

These bits select the number of levels for the TX_FIFO. They are effective only when the FIFOs are enabled. (See Table 7-16).

TABLE 7-16. TX_FIFO Size Encoding

TF_SIZ1	TF_SIZ0	FIFO Depth
0	0	16
0	1	32
1	x	Reserved

Bits 3,2 - RX_FIFO Size (RF_SIZ1,0)

These bits select the number of levels for the RX_FIFO. They are effective only when the FIFOs are enabled. (See Table 7-17).

TABLE 7-17. RX_FIFO Size Encoding

RF_SIZ1	RF_SIZ0	FIFO Depth
0	0	16
0	1	32
1	x	reserved

Bits 5,4 - Prescaler Select

The prescaler divides the 24 MHz input clock frequency to provide the clock for the baud rate generator. (See Table 7-18).

TABLE 7-18. Prescaler Select

Bit 5	Bit 4	Prescaler Value
0	0	13
0	1	1.625
1	0	Reserved
1	1	1.0

Bit 6 - Reserved

Read/write 0.

Bit 7 - Baud Rate Divisor Register Lock (LOCK)

When set to 1, accesses to the baud rate generator divisor register through LBGD(L) and LBGD(H) as well as fallback are disabled from non-extended mode.

In this case two scratchpad registers overlaid with LBGD(L) and LBGD(H) are enabled, and any attempted CPU access of the baud rate generator divisor register through LBGD(L) and LBGD(H) will access the scratchpad registers instead. This bit must be set to 0 when extended mode is selected.

7.15.5 Reserved Register, Bank 2, Offset 05h

Upon reset, all bits are set to 0.

Bits 7-0 - Reserved

Read/write 0's.

7.15.6 TX_FIFO Current Level Register (TXFLV), Bank 2, Offset 06h

This read-only register returns the number of bytes in the TX_FIFO. It can be used to facilitate programmed I/O modes during recovery from transmitter underrun in one of the fast infrared modes.

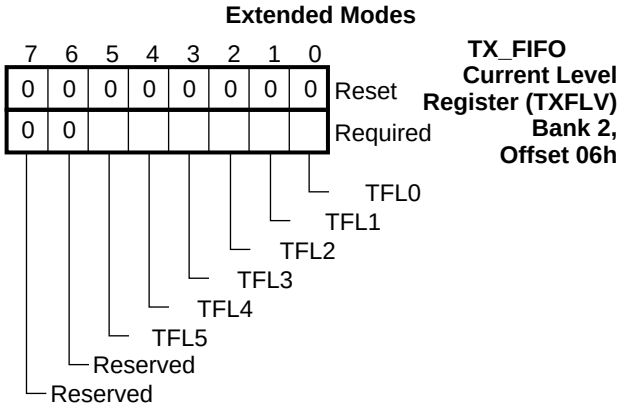


FIGURE 7-27. TXFLV Register Bitmap

Bits 5-0 - Number of Bytes in TX_FIFO (TFL(5-0))

These bits specify the number of bytes in the TX_FIFO.

Bits 7,6 - Reserved

Read/Write 0's.

7.15.7 RX_FIFO Current Level Register (RXFLV), IrDA or Consumer-IR Modes, Bank 2, Offset 07h

This read-only register returns the number of bytes in the RX_FIFO. It can be used for software debugging.

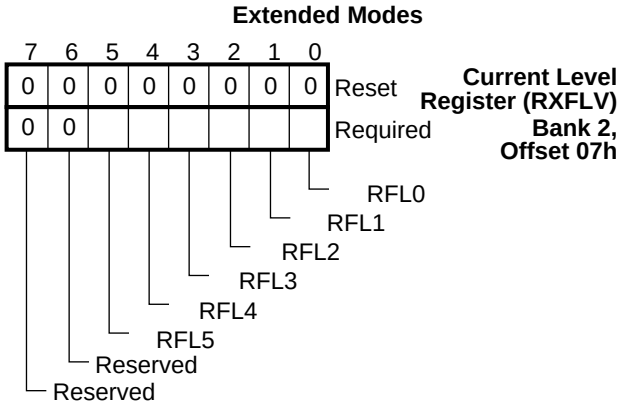


FIGURE 7-28. RXFLV Register Bitmap

Bits 5-0 - Number of Bytes in RX_FIFO (RFL(5-0))

These bits specify the number of bytes in the RX_FIFO.

Bits 7,6 - Reserved

Read/Write 0's.

Note: The contents of TXFLV and RXFLV are not frozen during CPU reads. Therefore, invalid data could be returned if the CPU reads these registers during normal transmitter and receiver operation. To obain correct data, the software should perform three consecutive reads and then take the data from the second read, if first and second read yield the same result, or from the third read, if first and second read yield different results.

7.16 BANK 3 – MODULE REVISION ID AND SHADOW REGISTERS

Bank 3 contains the Module Revision ID register which identifies the revision of the module, shadow registers for monitoring various registers whose contents are modified by being read, and status and control registers for handling the flow control.

TABLE 7-19. Bank 3 Register Set

Offset	Register Name	Description
00h	MRID	Module Revision ID Register
01h	SH_LCR	Shadow of LCR Register (Read Only)
02h	SH_FCR	Shadow of FIFO Control Register (Read Only)
03h	LCR/ BSR	Link Control Register/ Bank Select Register
04h-07h	Reserved	

7.16.1 Module Revision ID Register (MRID), Bank 3, Offset 00h

This read-only register identifies the revision of the module. When read, it returns the module ID and revision level. This module returns the code 2xh, where x indicates the revision number.

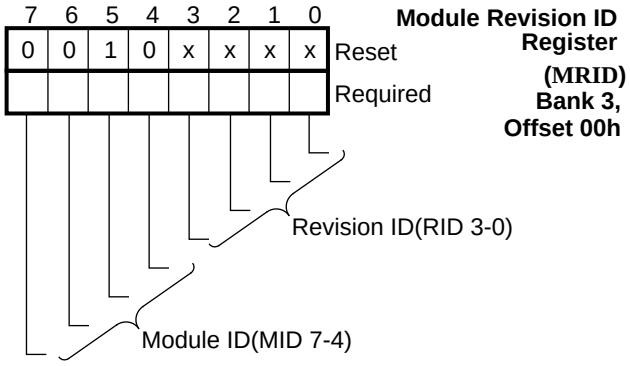


FIGURE 7-29. MRID Register Bitmap

Bits 3-0 - Revision ID (MID3-0)

The value in these bits identifies the revision level.

Bits 7-4 - Module ID (MID7-4)

The value in these bits identifies the module type.

7.16.2 Shadow of Link Control Register (SH_LCR), Bank 3, Offset 01h

This register returns the value of the LCR register. The LCR register is written into when a byte value according to Table 7-9 on page 123, is written to the LCR/BSR registers location (at offset 03h) from any bank.

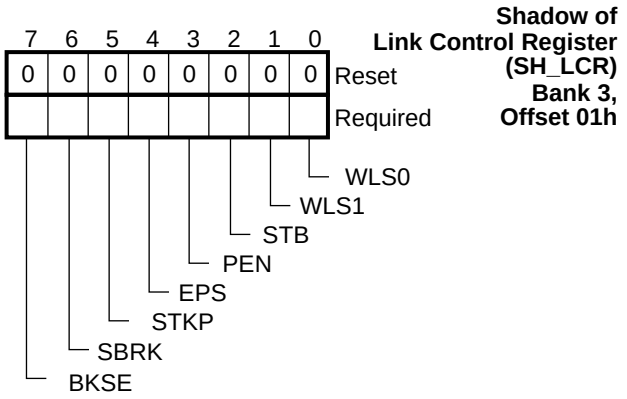


FIGURE 7-30. SH_LCR Register Bitmap

See "Link Control Register (LCR), All Banks, Offset 03h" on page 122 for bit descriptions.

7.16.3 Shadow of FIFO Control Register (SH_FCR), Bank 3, Offset 02h

This read-only register returns the contents of the FCR register in bank 0.

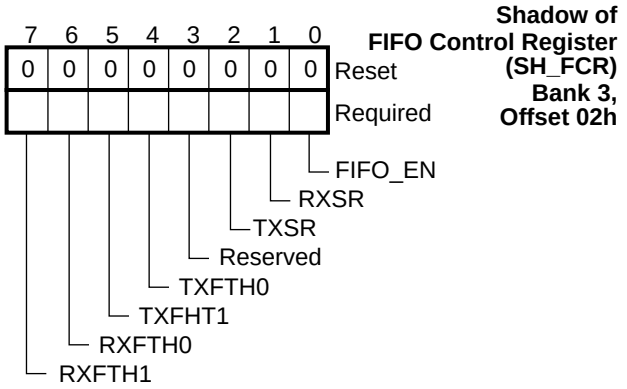


FIGURE 7-31. SH_LCR Register Bitmap

See "FIFO Control Register (FCR), Bank 0, Offset 02h" on page 121 for bit descriptions.

7.16.4 Link Control Register (LCR) and Bank Select Register (BSR), Bank 3, Offset 03h

These registers are the same as the registers at offset 03h in bank 0.

7.17 BANK 4 – TIMER AND FRAME BYTE COUNTERS

Bank 4 contains the Timer Reload Registers, as well as Frame Size Lengths and frame counters.

TABLE 7-20. Bank 4 Register Set

Offset	Register Name	Description
00h	TMR(L)	Timer Register (Low Byte)
01h	TMR(H)	Timer Register (High Byte)
02h	IRCR1	Infrared Control Register 1
03h	LCR/ BSR	Link Control/ Bank Select Registers
04h	TFRL(L)/ TFRCC(L)	Transmit Frame Length/ Current Count (Low Byte)
05h	TFRL(H)/ TFRCC(H)	Transmit Frame Length/ Current Count (High Byte)
06h	RFRML(L)/ RFRCC(L)	Receive Frame Maximum Length/ Current Count (Low Byte)
07h	RFRML(H)/ RFRCC(H)	Receive Frame Maximum Length/ Current Count (High Byte)

7.17.1 Interval Timer (TMR(L) and TMR(H)), Bank 4, Offsets 00h and 01h

This register is used to program the reload value for the internal down-counter as well as to read the current counter value. TMR is 12 bits wide and is split into two independently accessible parts occupying consecutive address locations.

TMR(L) is located at the lower address and accesses the least significant 8 bits, whereas TMR(H) is located at the higher address and accesses the most significant 4 bits. Values from 1 to 2^{12}- 1 can be used. The zero value is reserved and must not be used. The upper 4 bits of TMR(H) are reserved and must be written with 0's. The timer resolution is 125µs, providing a maximum timeout interval of approximately 0.5 seconds. To properly program the timer, the CPU must always write the lower value into TMR(L) first, and then the upper value into TMR(H). Writing into TMR(H) causes the counter to be loaded. A read of TMR returns the current counter value if the CTEST bit is 0, or the programmed reload value if CTEST is 1.

In order for a read access to return an accurate value, the CPU should always read TMR(L) first, and then TMR(H). This is because a read of TMR(H) returns the content of an internal latch that is loaded with the 4 most significant bits of the current counter value when TMR(L) is read.

After reset, the content of this register is indeterminate.

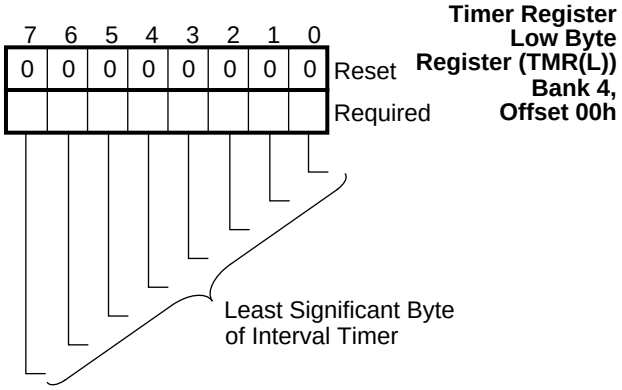


FIGURE 7-32. TMR(L) Register Bitmap

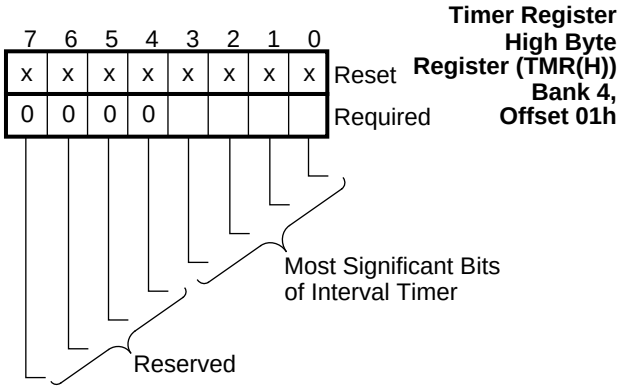


FIGURE 7-33. TMR(H) Register Bitmap

7.17.2 Infrared Control Register 1 (IRCR1), Bank 4, Offset 02h

Controls the timer and counters, and enables the Sharp-IR or SIR infrared mode in the Non-Extended mode of operation.

Upon reset, all bits are set to 0.

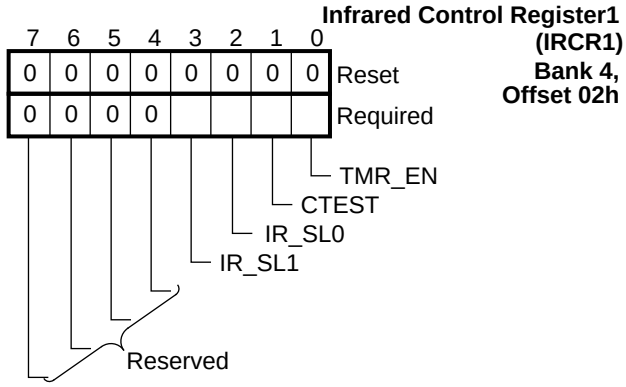


FIGURE 7-34. IRCR1 Register Bitmap

Bit 0 - Timer Enable (TMR_EN)

Enables the timer.

0 - Timer is frozen. (Default)

1 - Timer is enabled.

Bit 1 - Counter Test (CTEST)

When this bit is set to 1, the TMR register reload value, as well as the TFRL and RFRML register contents are returned during CPU reads

Bits 3,2 - Sharp-IR or SIR Mode Select (IR_SL1,0), Non-Extended Mode Only

These bits enable Sharp-IR and SIR modes in Non-Extended mode. They allow selection of the appropriate infrared interface when Extended mode is not selected. These bits are ignored when Extended mode is selected. Before running the legacy application in Sharp-IR or SIR Mode, run a small enabling routine to set bits 3 and 2 to the appropriate mode, i.e., 10 or 11 (see Table 7-21). The infrared application can then be executed and this module will be pre-set for the appropriate mode.

Upon termination of the application these bits should be reset to 00 to switch back to a UART mode.

TABLE 7-21. Sharp-IR or SIR Mode Selection

IR_SL1	IR_SL0	Selected Mode
0	0	UART (Default)
0	1	Reserved
1	0	Sharp-IR
1	1	SIR

Bits 7-4 - Reserved

Read/Write 0.

7.17.3 Link Control Register (LCR) and Bank Select Register (BSR), Bank 4, Offset 03h

These registers are the same as the registers at offset 03h in bank 0.

7.17.4 Transmission Frame Length Register (TFRL) or Transmission Frame Current Count Register (TFRCC), Bank 4, Offsets 04h and 05h

These registers share the same addresses.

TFRL is always accessed during write cycles and is used to program the transmitted frame length (in bytes) for the frame to be transmitted. The frame length value does not include appended CRC bytes. TFRL is accessed during read cycles, if the CTEST bit is set to 1, and returns the previously programmed value. Values from 1 to 2^{13} - 1 are valid. The zero value is reserved and must not be used.

TFRCC is loaded with the content of TFRL when transmission of a frame begins, and decrements after each byte is transmitted. It is read-only and is accessed when the CTEST bit is 0. It returns the number of currently remaining bytes of the frame being transmitted.

These registers are 13 bits wide and are split into two independently accessible parts occupying consecutive address locations. TFRL(L) and TFRCC(L) are located at the lower

address and access the least significant eight bits, whereas TFRL(H) and TFRCC(H) are located at the higher address and access the most significant five bits. The upper three bits of TFRL(H) are reserved and 0's must be written to them.

In order for a read access of TFRCC to return an accurate value, the CPU should always read TFRCC(L) first, and than read TFRCC(H).

After reset, the content of the TFRL register is 800h.

To properly program TFRL, the CPU must always write the lower value into TFRL(L) first, and then the upper value into TFRL(H).

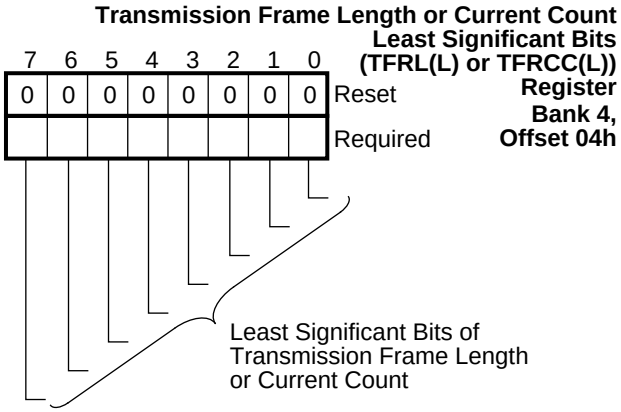


FIGURE 7-35. TFRL(L) or TFRCC(L) Register Bitmap

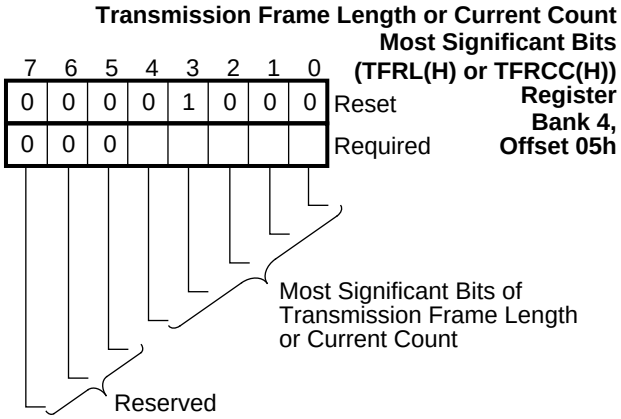


FIGURE 7-36. TFRL(H) or TFRCC(H) Register Bitmap

Note: TFRCC is for testing purposes only.

7.17.5 Reception Frame Maximum Length (RFRML) or Reception Frame Current Count (RFRCC) Registers, Bank 4, Offsets 06h and 07h

These registers share the same addresses.

RFRML is always accessed during write cycles and is used to program the maximum frame length (in bytes) for the frame to be received. The maximum frame length value includes the CRC bytes. RFRML is accessed during read cycles, if the CTEST bit is set to 1, and returns the previously programmed value. Values from 1 to $2^{13} - 1$ can be used. The zero value is reserved and must not be used.

RFRCC is set to 0 when reception of a frame begins, and increments after each byte is received. It is read-only and is accessed during CPU read cycles when the CTEST bit is 0. It returns the current number of bytes of the frame being received.

These registers are 13 bits wide and are split into two independently accessible parts at consecutive addresses.

RFRML(L) and RFRCC(L) are at the lower addresses and access the least significant eight bits, whereas RFRML(H) and RFRCC(H) are at the higher addresses and access the most significant five bits. The upper three bits of RFRML(H) are reserved and must be 0.

In order for a read access of RFRCC to return an accurate value, the CPU should always read RFRCC(L) following a read of RFRCC(H).

After reset, the content of the RFRML register is 800h.

To properly program RFRML, the CPU must always write the lower value into RFRML(L) first, and then the upper value into RFRML(H).

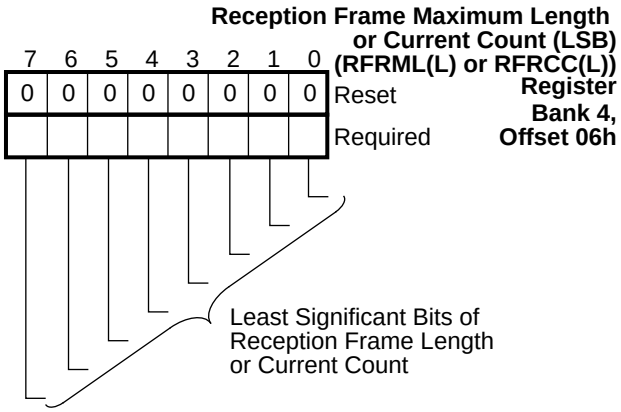


FIGURE 7-37. RFRML(L) or RFRCC(L) Register Bitmap

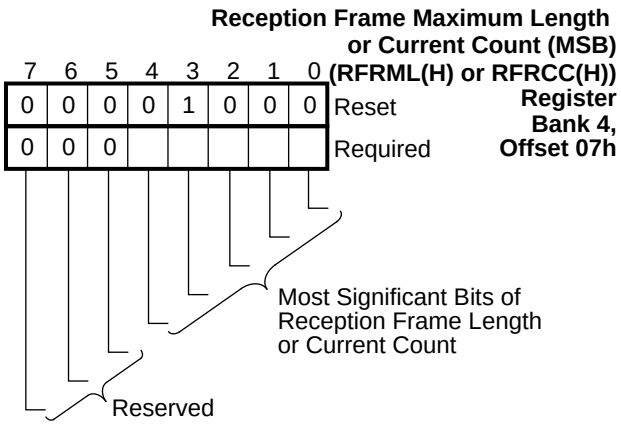


FIGURE 7-38. RFRML(H) or RFRCC(H) Register Bitmap

Note: RFRCC is for testing purposes only.

7.18 BANK 5 – INFRARED CONTROL AND ST_FIFO REGISTERS

The registers in this bank handle pipelining, infrared control and ST_FIFO parameters. For information about the pipeline operation see ”Pipelining” on page 115.

TABLE 7-22. Bank 5 Registers

Offset	Register Name	Description
00h	P_BGD(L)	Pipelined Baud Rate Generator Divisor, Low Byte
01h	P_BGD(H)	Pipelined Baud Rate Generator Divisor, High Byte
02h	P_MDR	Pipeline Mode Register
03h	LCR/ BSR	Link Control Register/ Bank Select Register
04h	IRCR2	Infrared Control Register 2
05h	FRM_ST	Frame Status
06h	RFRL(L)/ LSTFRC	Received Frame Length at Bottom of ST_FIFO (Low Byte)/Lost Frame Count
07h	RFRL(H)	Received Frame Length at Bottom of ST_FIFO (High Byte)

7.18.1 Pipelined Baud Rate Generator Divisor Registers, (P_BGD(L) and P_BGD(H)), Bank 5, Offsets 00h and 01h

The Pipeline Baud Rate Generator Divisor (P_BGD(L) and P_BGD(H)) registers hold the 16-bit value that determines the new baud rate following a pipeline operation. These registers occupy consecutive address locations.

The value written into these registers is loaded into the least and most significant parts of the baud rate generator divisor register when the transmitter becomes empty and both the MD_PEN and BR_PEN bits in the P_MDR register are set to 1.

Upon reset, the content of these registers is indeterminate.

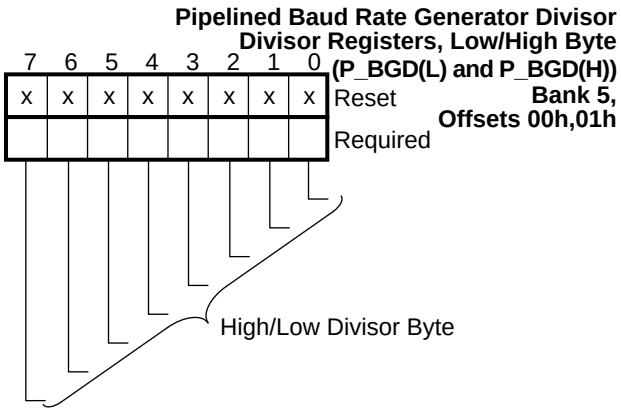


FIGURE 7-39. Pipelined Baud Rate Generator Divisor Register Bitmap

7.18.2 Pipeline Mode Register (P_MDR), Bank 5, Offset 02h

The Pipeline Mode Register can be read or written in any mode. However, a pipeline operation will only take place if the current operation mode and next operation mode are both IrDA modes. Furthermore, SIR must be selected in extended mode and the TX_FIFO must be enabled.

When a pipeline operation takes place, the following occurs:

1. If the target mode is MIR or FIR, the transmitter is halted for 250µs.
2. If the target mode is SIR, the transmitter is halted for 250µs or for a character time (at the newly selected baud rate), whichever is greater.

Upon reset, all bits are set to 0.

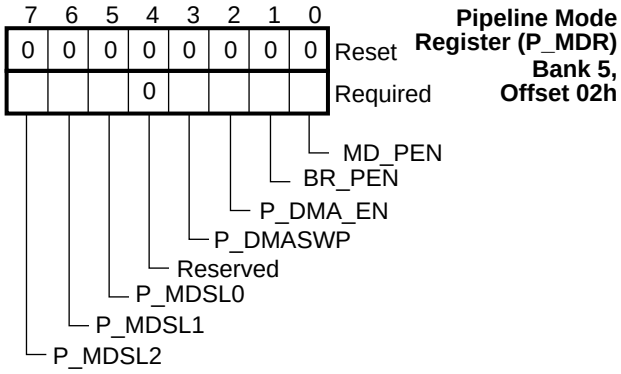


FIGURE 7-40. P_MDR Register Bitmap

Bit 0 - Mode Bits Pipeline Enable (MD_PEN)

When set to 1, a pipeline load operation takes place when the transmitter becomes empty. Bits 7, 6, 5 and 2 are loaded into the corresponding bit positions in the MCR (see page 123), and bit 3 is loaded into bit position 3 of EXCR1 (see page 130).

This bit is automatically cleared after the load has occurred and the pipeline status bit in the ASCR (see page 127) is set, indicating that a pipeline event occurred. If pipeline interrupts are enabled, then an interrupt is generated.

Bit 1 - Baud Rate Pipeline Enable (BR_PEN)

This bit is effective only when the MD_PEN bit (bit 0) is set to 1. If the transmitter becomes empty while this bit set to 1, the P_BGD register will be loaded into the baud rate generator divisor register.

Bit 2 - Pipelined DMA Enable (P_DMA_EN)

When pipelining is enabled, whenever the transmitter becomes empty this bit will be placed in the DMA Enable bit in the Modem Control Register (MCR), thereby enabling/disabling DMA as is appropriate for the next mode of operation.

Bit 3 - Pipelined DMA Swap (P_DMASWP)

When pipelining is enabled, this bit Indicates a swap is pending on the DMA channel. Whenever the transmitter becomes empty, this bit is placed in the DMA swap bit in the Modem Control Register (MCR), thereby enabling

or disabling DMA input and output switching on the same channel, when 8237 type DMA is used, as is appropriate for the next mode of operation.

Bit 4 - Reserved

Read/Write 0.

Bits 7-5 - Pipelined Mode Select Bits (PMDSL2-0)

When MD_PEN is enabled and the transmitter becomes empty, these bits are copied into their respective bits in the Modem Control Register (MCR).

7.18.3 (LCR/BSR) Register, Bank 5, Offset 03h

These registers are the same as the registers at offset 03h in bank 0.

7.18.4 Infrared Control Register 2 (IRCR2), Bank 5, Offset 04h

This register controls the basic settings of the infrared modes.

Upon reset, the content of this register is 02h.

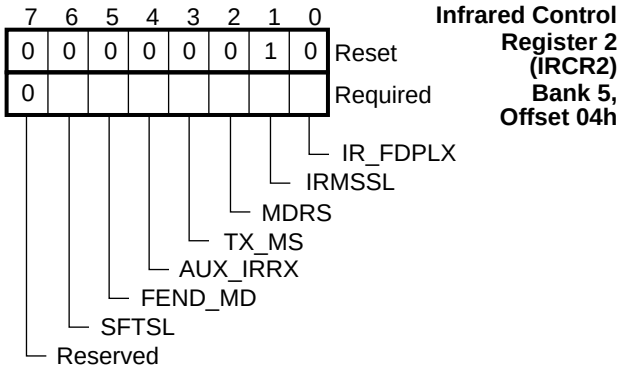


FIGURE 7-41. IRCR2 Register Bitmap

Bit 0 - Enable Infrared Full Duplex Mode (IR_FDPLX)

When set to 1, the infrared receiver is not masked during transmission.

Bit 1 - MSR Register Function Select in Infrared Mode (IRMSSL)

This bit selects the behavior of the Modem Status Register (MSR) and the Modem Status Interrupt (MS_EV) when any infrared mode is selected. When a UART mode is selected, the Modem Status Register and the Modem Status Interrupt function normally, and this bit is ignored.

0 - MSR register and modem status interrupt work in the IR modes as in the UART mode (Enables external circuitry to perform carrier detection and provide wake-up events).

1 - The MSR returns 30h, and the Modem Status Interrupt is disabled. (Default)

Bit 2 - MIR Data Rate Select (MDRS)

This bit determines the data rate in MIR mode.

0 - 1.152 Mbps (default)

1 - 0.576 Mbps

Bit 3 - Transmitter Mode Select (TX_MS)

This bit is used in MIR and FIR modes only.

When it is set to 1, transmitter frame-end stop mode is selected.

In this case the transmitter stops after transmission of a frame is complete, if the end-of-frame condition was generated by the TFRCC counter reaching 0.

The transmitter can be restarted by clearing the TXHFE bit in the ASCR (see page 127).

Bit 4 - Auxiliary Infrared Input Select (AUX_IRRX)

When set to 1, the infrared signal is received from the auxiliary input (Separate input signals may be desired for different front-end circuits). See Table 7-35 on page 148.

Bit 5 - Frame End Mode Control (FEND_MD)

This bit selects whether a Terminal-Count(TC) condition from the TFRCC register (see on page 135) will generate an EOF in PIO mode or in DMA mode.

0 - TFRCC terminal count effective in PIO mode.

1 - TFRCC terminal count effective in DMA mode.

For a complete discussion of back-to-back frame transmission refer to ”High-Speed Infrared Transmission” on page 111.

Bit 6 - ST_FIFO Threshold Select (SFTSL)

An interrupt request is generated when the ST_FIFO level reaches the threshold or when an ST_FIFO timeout occurs.

TABLE 7-23. ST_FIFO Interrupt Threshold Levels

SFTSL Bit Value	Threshold Level
0	2
1	4

Bit 7 - Reserved

Read/Write 0.

7.18.5 The ST_FIFO

An 8-level ST_FIFO is used in **MIR** and **FIR** modes to support back-to-back incoming frames when the DMA is enabled and an 8237-type DMA controller is used.

Each ST_FIFO entry contains either status information and frame length for a single frame, or the number of lost frames.

The bottom entry spans three address locations, and is accessed via the following three registers (FRM_ST, RFRL(L)/LSTFRC and RFRL(H)).

The ST_FIFO is flushed when a reset occurs or when the operational mode is changed.

Status and length data are loaded into the ST_FIFO whenever the DMA_EN bit in the extended-mode MCR register is set to 1 and an 8237-type DMA controller is used, regardless of whether the CPU or the DMA controller is transferring the data from the RX_FIFO to memory. This implies that, during testing, if full duplex is enabled and a DMA channel is servicing the transmitter while the CPU is servic-

ing the receiver, the CPU must still read the ST_FIFO otherwise the ST_FIFO can be filled up and incoming frames will be rejected.

7.18.6 Frame Status at FIFO Bottom Register (FRM_ST), Bank 5, Offset 05h

This read-only register returns the status byte at the bottom of the frame ST_FIFO. The ST_FIFO and the received frame length can be used to determine the validity and the position of the received frames inside the reception buffer.

If the LOST_FR bit is 0, bits 0 to 4 indicate if any error condition occurred during reception of the corresponding frame. Error conditions also affect the error flags in the LSR register.

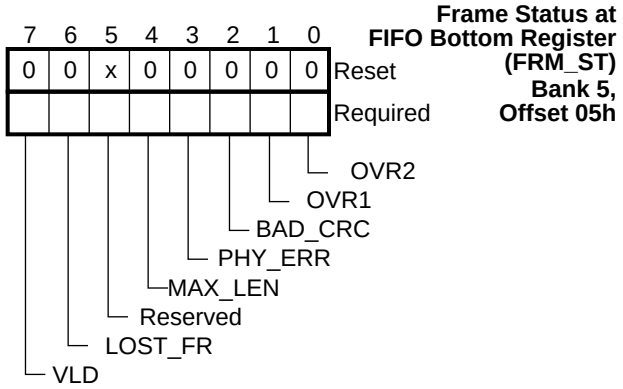


FIGURE 7-42. FRM_ST Register Bitmap

Bit 0 - Overrun Error 2 (OVR2)

This bit is set to 1 when incoming characters or entire frames have been discarded due to the ST_FIFO being full.

Bit 1 - Overrun 1 (OVR1)

This bit is set to 1 when incoming characters or entire frames have been discarded due to the RX_FIFO being full.

Bit 2 - CRC Error (BAD_CRC)

This bit is set to 1 when a mismatch between the received CRC and the receiver-generated CRC is detected.

Bit 3 - Physical Layer Error (PHY_ERR)

This bit is set to 1 when an encoding error or the sequence BOF-data-BOF is detected in FIR mode, or an abort condition is detected in MIR mode.

Bit 4 - Maximum Length Exceeded (MAX_LEN)

This bit is set to 1 when a frame exceeding the maximum length has been received. The extra bytes are discarded (they are not stored).

Bit 5 - Reserved

Returned data is indeterminate.

Bit 6 - Lost Frame Indicator Flag (LOST_FR)

Indicates the type of information provided by this entry.

0 - Entry provides status information and length for a received frame.

1 - Entry provides overrun indications and number of lost frames.

Bit 7 - ST_FIFO Valid (VLD)

When set to 1, indicates that the bottom entry in the ST_FIFO contains valid data.

7.18.7 Received Frame Length LSB (RFRL(L)) or Lost Frame Count at ST_FIFO Bottom (LSTFRC), Bank 5, Offset 06h

This read-only register should only be read when the VLD bit (bit 7) in the Frame ST_FIFO Bottom (FRM_ST) register is 1 (See previous section). The information returned depends on the setting of the LOST_FR bit (bit 6 in the FRM_ST register).

When the LOST_FR bit is 0, this register contains the eight least significant bits of the received frame length.

When the LOST_FR bit is 1, the register contains the number of lost frames.

Upon reset, all bits are undefined.

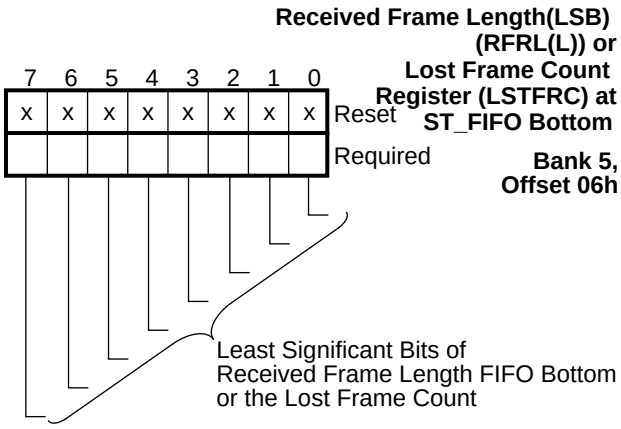


FIGURE 7-43. RFRL(L) or LSTFRC Register Bitmap

7.18.8 Received Frame Length (MSB) at ST_FIFO Bottom (RFRL(H)), Bank 5, Offset 07h

This read-only register should only be read when the VLD bit in FRM_ST is 1. The information returned depends on the setting of the LOST_FR bit (bit 6 in the FRM_ST register).

When the LOST_FR bit is zero, the register contains the most significant 5 bits of the received frame length.

When the LOST_FR bit is one, all bits are set to 0.

Reading this register removes the bottom ST_FIFO entry.

Upon reset, all bits are set to 0.

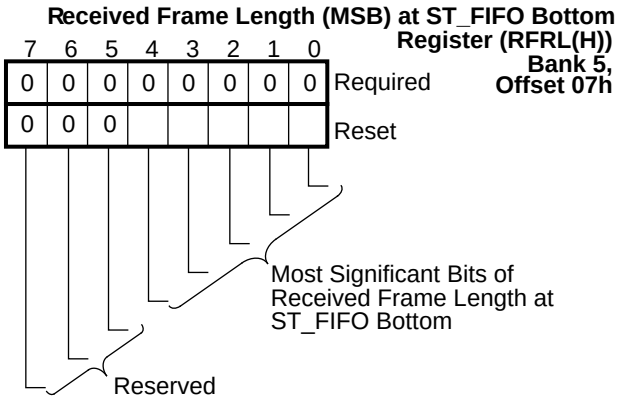


FIGURE 7-44. RFRL(H) Register Bitmap

7.19 BANK 6 – INFRARED PHYSICAL LAYER CONFIGURATION REGISTERS

This Bank of registers controls aspects of the framing and timing of the infrared modes.

TABLE 7-24. Bank 6 Register Set

Offset	Register Name	Description
00h	IRCR3	Infrared Control Register 3
01h	MIR_PW	MIR Pulse Width Control (1.152 Mbps)
02h	SIR_PW	SIR Pulse Width Control (≤ 115 Kbps)
03h	LCR/ BSR	Link Control Register/ Bank Select Register
04h	BFPL	Beginning Flags and Preamble Length Register
05h - 07h	Reserved	

7.19.1 Infrared Control Register 3 (IRCR3), Bank 6, Offset 00h

This Register selects the operating mode of the infrared interface. It also designates the CRC used for that mode and enables/disables modulation in Sharp-IR mode.

To facilitate testing of the internal circuitry or confirm the status of a connection in the High Speed IrDA modes (MIR and FIR), the CRC may be inverted or disabled to intentionally insert errors into the data stream.

To facilitate custom modes of operation the CRC is selectable. Typically, MIR uses CRC-16, and FIR uses CRC-32.

Upon reset, the content of this register is 20h.

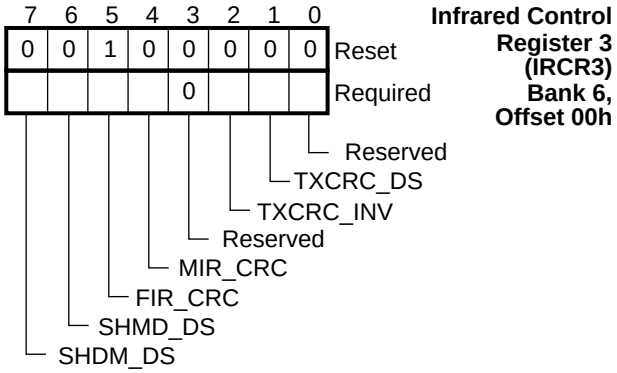


FIGURE 7-45. IRCR3 Register Bitmap

Bit 0 - Reserved

Read/Write 0.

Bit 1 - Disable Transmitter CRC (TXCRC_DS)

0 - Append CRC to frames in the **MIR** and **FIR** modes of operation. (Default).

1 - CRC is not transmitted.

Bit 2 - Invert Transmitter CRC (TXCRC_INV)

When set to 1, an inverted CRC is transmitted (This bit can be used to force a bad CRC to be sent to test the datalink).

0 - Send CRC normally. (Default).

1 - Invert CRC.

Bit 3 - Reserved

Read/Write 0.

Bit 4 - MIR Mode CRC Select (MIR_CRC)

Selects the CRC length in 1.152 Mbps (MIR) mode.

0 - 16-bit CRC. (Default)

1 - 32-bit CRC.

Bit 5 - FIR Mode CRC Select (FIR_CRC)

Selects the CRC length in 4.0 Mbps (FIR) mode.

0 - 16 Bit CRC.

1 - 32 Bit CRC. (Default)

Bit 6 - Sharp-IR Modulation Disable (SHMD_DS)

0 - Enables internal 500KHz transmitter modulation. (Default)

1 - Disables internal modulation.

Bit 7 - Sharp-IR Demodulation Disable (SHDM_DS)

0 - Enables internal 500 KHz receiver demodulation. (Default)

1 - Disables internal demodulation.

7.19.2 MIR Pulse Width Register (MIR_PW), Bank 6, Offset 01h

This register sets the pulse width for transmitted MIR operation mode infrared pulses in increments of 20.83 or 41.666 nsec, depending on the setting of the MDRS bit in the IRCR2 Register (see p.138). These setting do not affect the receiver.

Upon reset, this register is set to 0Ah.

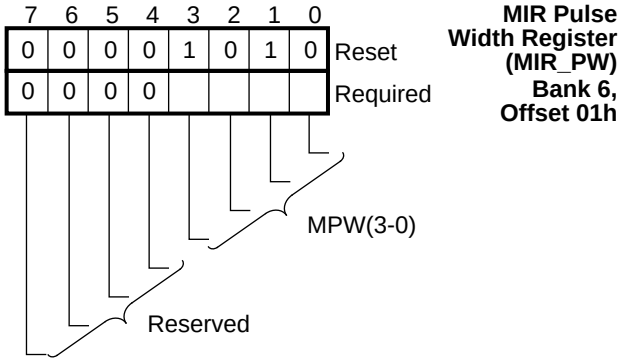


FIGURE 7-46. MIR_PW Register Bitmap

Bits 3-0 - MIR Pulse Width Register (MPW)

These bits specify the pulse width in nsec, for MIR mode (see Table 7-25). Each bit increments the pulse width by 20.83 nsec or 41.666 nsec according to the MDRS bit in IRCR2 (see page 138).

TABLE 7-25. MIR Pulse width Settings

ENCODING MPW Bits 3-0	Pulse Width MDRS = 0	Pulse Width MDRS = 1
00XX	Reserved	Reserved
0100	83.33ns	166.66ns
0101	104.16ns	208.33ns
0110	125ns	250ns
0111	145.83ns	291.66ns
1000	166.66ns	333.33ns
1001	187.50ns	374.99ns
1010	208.33ns	416.66ns
1011	229.16ns	458.33
1100	250ns	500ns
1101	270.83ns	541.66ns
1110	291.66ns	583.32ns
1111	312.5ns	625ns

Bits 7-4 - Reserved

Read/Write 0's.

7.19.3 SIR Pulse Width Register (SIR_PW), Bank 6, Offset 02h

This register sets the pulse width for transmitted pulses in SIR operation mode. These setting do not affect the receiver. Upon reset, the content of this register is 00h, which defaults to a pulse width of 3/16 of the baud rate.

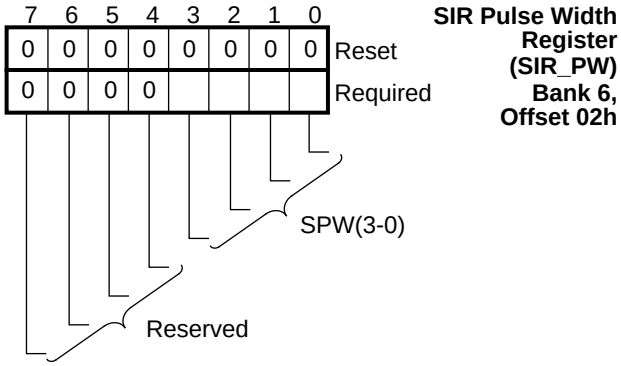


FIGURE 7-47. SIR_PW Register Bitmap

Bits 3-0 - SIR Pulse Width Register (SPW)

Two codes for setting the pulse width are available. All other values for this field are reserved.

0000 - Pulse width is 3/16 of the bit period. (Default)

1101 - Pulse width is 1.6 µsec.

Bits 7-4 - Reserved

Read/Write 0's.

7.19.4 Link Control Register (LCR) and Bank Select Register (BSR), Bank 6, Offset 03h

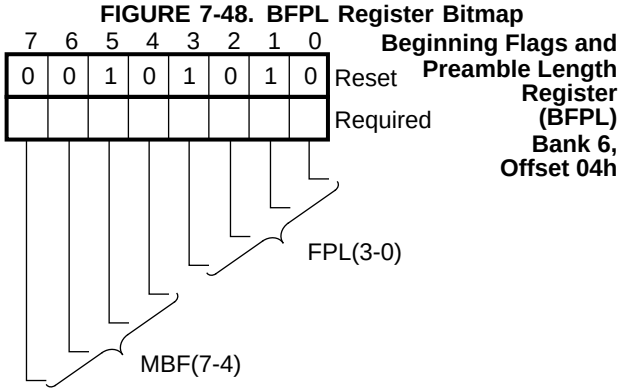
These registers are the same as the registers at offset 03h in Bank 0.

7.19.5 Beginning Flags and Preamble Length Register (BFPL), Bank 6, Offset 04h

This register programs the number of beginning flags for **MIR** mode and the preamble bytes for the **FIR** mode.

This register defaults to 2Ah, selecting two beginning flags for MIR mode and 16 preamble symbols for FIR mode.

FIGURE 7-48. BFPL Register Bitmap



Bits 3-0 - FIR Preamble Length (in bytes) (FPL(3-0))

Selects the number of preamble symbols for **FIR** frames.

Table 7-26 specify the number of preamble symbols for **FIR** frames.

TABLE 7-26. FIR Preamble Length

ENCODING FPL Bits (3-0)	Preamble Length (in Bytes)
0000	Reserved
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	8
1000	10
1001	12
1010	16 (Default)
1011	20
1100	24
1101	28
1110	32
1111	Reserved

Bits 7-4 - MIR Beginning Flags (MBF(3-0))

Selects the number of beginning flags for **MIR** frames.

Table 7-27 specify the number of beginning of flags for **MIR** frames.

TABLE 7-27. MIR Beginning Flags

ENCODING MBF Bits (3-0)	Beginning Flags
0000	Reserved
0001	1
0010	2 (Default)
0011	3
0100	4
0101	5
0110	6
0111	8
1000	10
1001	12
1010	16
1011	20
1100	24
1101	28
1110	32
1111	Reserved

7.20 BANK 7 – CONSUMER-IR AND OPTICAL TRANSCEIVER CONFIGURATION REGISTERS

Bank 7 contains the registers that configure Consumer-IR functions and infrared transceiver controls. See Table 7-28.

TABLE 7-28. Bank 7 Register Set

Offset	Register Name	Description
00h	IRRXDC	Infrared Receiver Demodulator Control Register
01h	IRTXMC	Infrared Transmitter Modulator Control Register
02h	RCCFG	Consumer-IR Configuration Register
03h	LCR/BSR	Link Control Register/ Bank Select Register
04h	IRCFG1	Infrared Interface Configuration Register 1
05h	IRCFG2	Infrared Interface Configuration Register 2
06h	IRCFG3	Infrared Interface Configuration Register 3
07h	IRCFG4	Infrared Interface Configuration Register 4

The Consumer-IR utilizes two carrier frequency ranges (see also Table 7-32):

- Low range which spans from 30 KHz to 56 KHz, in 1 KHz increments, and
- High range which includes three frequencies: 400KHz, 450KHz or 480KHz.

High and low frequencies are specified independently to allow separate transmission and reception modulation settings. The transmitter uses the carrier frequency settings in Table 7-32.

The four registers at offsets 04h through 07h (the infrared transceiver configuration registers) are provided to configure the Infrared Interface (the transceiver). The transceiver mode is selected by up to three special output signals

(IRSL2-0). When programmed as outputs these signals are forced to low when automatic configuration is enabled (AMCFG bit set to 1) and a UART mode is selected.

7.20.1 Infrared Receiver Demodulator Control Register (IRRXDC), Bank 7, Offset 0

This register controls settings for Sharp-IR and Consumer IR reception. After reset, the content of this register is 29h. This setting selects a subcarrier frequency in a range between 34.61 KHz and 38.26 KHz for the Consumer-IR mode, and from 480.0 to 533.3 KHz for the Sharp-IR mode. The value of this register is ignored in both modes if the receiver demodulator is disabled. The available frequency ranges for Consumer-IR and Sharp-IR modes are given in Tables 7-29 through 7-31.

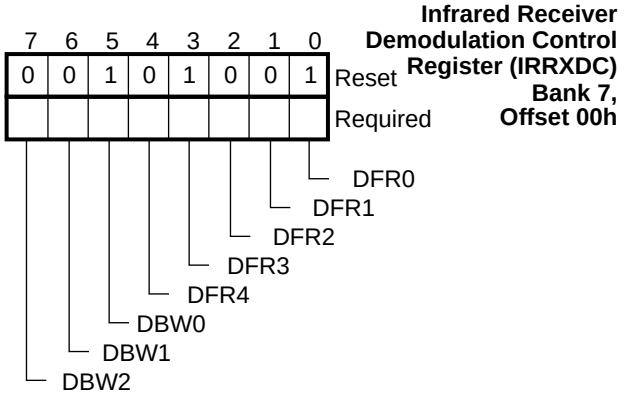


FIGURE 7-49. IRRXDC Register Bitmap

Bits 4-0 - Demodulator Frequency (DFR(4-0))

These bits select the subcarrier's center frequency for the Consumer-IR receiver demodulator. Table 7-29 shows the selection for low speed demodulation (bit 5 of RCCFG=0, see page 146), and Table 7-30 shows the selection for high speed demodulation (bit 5 of RCCFG=1).

Bits 7-5 - Demodulator Bandwidth (DBW(2-0))

These bits set the demodulator bandwidth for the selected frequency range. The subcarrier signal frequency must fall within the specified frequency range in order to be accepted. Used for both Sharp-IR and Consumer-IR modes.

See Tables 7-29, 7-30 and bit 5 (RXHSC) of the Consumer-IR Configuration (RCCFG) Register on page 146.

7.20.2 Infrared Transmitter Modulator Control Register (IRTXMC), Bank 7, Offset 01h

This register controls modulation subcarrier parameters for Consumer-IR and Sharp-IR mode transmission. For Sharp-IR, only the carrier pulse width is controlled by this register - the carrier frequency is fixed at 500 KHz.

After reset, the value of this register is 69h, selecting a carrier frequency of 36 KHZ and an IR pulse width of 7 µsec for Consumer-IR, or a pulse width of 0.8 µsec for Sharp-IR.

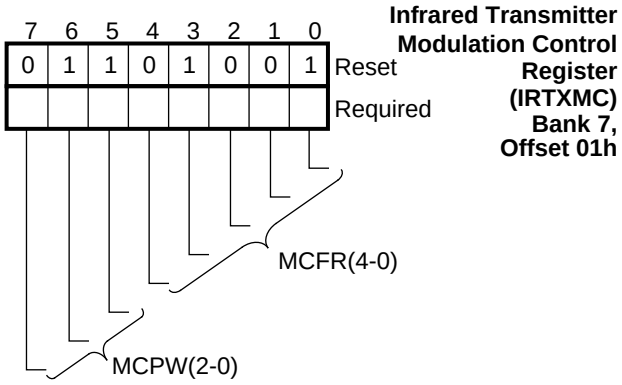


FIGURE 7-50. IRTXMC Register Bitmap

Bits 4-0 - Modulation Subcarrier Frequency (MCFR)

These bits set the frequency for the Consumer-IR modulation subcarrier. The encoding are defined in Table 7-32. Bits 7-5 - Modulation Subcarrier Pulse Width (MCPW)

Specify the pulse width of the subcarrier clock as shown in Table 7-33.

TABLE 7-29. Consumer-IR, Low Speed Demodulator (RXHSC = 0) (Frequency Ranges in kHz)

DFR Bits 4 3 2 1 0	DBW2-0 (Bits 7, 6 and 5 of IRRXDC)						
	min/max	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0
0 0 0 1 0	min	26.66	25.45	24.34	23.33	22.40	21.53
	max	29.47	31.11	32.94	35.00	37.33	40.00
0 0 0 1 1	min	28.57	27.27	26.08	25.00	24.00	23.07
	max	31.57	33.33	35.29	37.50	40.00	42.85
0 0 1 0 0	min	29.28	27.95	26.73	25.62	24.60	23.65
	max	32.37	34.16	36.17	38.43	41.00	43.92
0 0 1 0 1	min	30.07	28.68	27.43	26.29	25.24	24.27
	max	33.24	35.05	37.11	39.43	42.06	45.07
0 0 1 1 0	min	31.74	30.30	28.98	27.77	26.66	25.63
	max	35.08	37.03	39.21	41.66	44.44	47.61
0 0 1 1 1	min	32.60	31.13	29.78	28.54	27.40	26.34
	max	36.00	38.05	40.29	42.81	45.66	48.92
0 1 0 0 0	min	33.57	32.04	30.65	29.37	28.20	27.11
	max	37.10	39.16	41.47	44.06	47.00	50.35
0 1 0 0 1	min	34.61	33.04	31.60	30.29	29.08	27.96
	max	38.26	40.38	42.76	45.43	48.46	51.92
0 1 0 1 0	min	35.71	34.09	32.60	31.25	30.00	28.84
	max	39.47	41.66	44.11	46.87	50.00	53.57
0 1 0 1 1	min	36.85	35.18	33.65	32.25	30.96	29.76
	max	40.73	43.00	45.52	48.37	51.60	55.28
0 1 1 0 0	min	38.10	36.36	34.78	33.33	32.00	30.77
	max	42.10	44.44	47.05	50.00	53.33	57.14
0 1 1 0 1	min	39.40	37.59	36.00	34.45	33.08	31.80
	max	43.55	45.94	48.64	51.68	55.13	59.07
0 1 1 1 0	min	40.81	38.95	37.26	35.70	34.28	32.96
	max	45.11	47.61	50.41	53.56	57.13	61.21
1 0 0 1 0	min	42.32	40.40	38.64	37.03	35.55	34.18
	max	46.78	49.37	52.28	55.55	59.25	63.48
1 0 0 1 1	min	43.95	41.95	40.13	38.45	36.92	35.50
	max	48.58	51.27	54.29	57.68	61.53	65.92
1 0 1 0 1	min	45.71	43.63	41.74	40.00	38.40	36.92
	max	50.52	53.33	56.47	60.00	64.00	68.57
1 0 1 1 1	min	47.62	45.45	43.47	41.66	40.00	38.46
	max	52.63	55.55	58.82	62.50	66.66	71.42
1 1 0 1 0	min	49.66	47.40	45.34	43.45	41.72	40.11
	max	54.90	57.94	61.35	65.18	69.53	74.50
1 1 0 1 1	min	51.90	49.54	47.39	45.41	43.60	41.92
	max	57.36	60.55	64.11	68.12	72.66	77.85
1 1 1 0 1	min	54.38	51.90	49.65	47.58	45.68	43.92
	max	60.10	63.44	67.17	71.37	76.13	81.57

TABLE 7-30. Consumer IR, High Speed Demodulator (RXHSC = 1) (Frequency Ranges in kHz)

DFR Bits 4 3 2 1 0	DBW2-0 (Bits 7, 6 and 5 of IRRXDC)						
	min/max	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0
0 0 0 1 1	min	380.95	363.63	347.82	333.33	320.00	307.69
	max	421.05	444.44	470.58	500.00	533.33	571.42
0 1 0 0 0	min	436.36	417.39	400.00	384.00	369.23	355.55
	max	480.00	505.26	533.33	564.70	600.00	640.00
0 1 0 1 1	min	457.71	436.36	417.39	400.00	384.00	369.92
	max	502.26	533.33	564.70	600.00	640.00	685.57

TABLE 7-31. Sharp-IR Demodulator (Frequency Ranges in kHz)

DFR Bits 4 3 2 1 0	DBW2-0 (Bits 7, 6 and 5 of IRRXDC)						
	min/max	001	010	011	100	101	110
x x x x x x	min	480.0	457.1	436.4	417.4	400.0	384.0
	max	533.3	564.7	600.0	640.0	685.6	738.5

TABLE 7-32. Consumer-IR Carrier Frequency Encoding

Encoding MCFR Bits 43210	Low Frequency (TXHSC = 0)	High Frequency (TXHSC = 1)
00000	reserved	reserved
00001	reserved	reserved
00010	reserved	reserved
00011	30 KHz	400 KHz
00100	31 KHz	reserved
00101	32 KHz	reserved
00110	33 KHz	reserved
00111	34 KHz	reserved
01000	35 KHz	450 KHz
01001	36 KHz	reserved
01010	37 KHz	reserved
01011	38 KHz	480 KHz
01100	39 KHz	reserved
01101	40 KHz	reserved
01110	41 KHz	reserved
. . .	. . .	. . .
11010	53 KHz	reserved
11011	54 KHz	reserved
11100	55 KHz	reserved
11101	56 KHz	reserved
11110	56.9 KHz	reserved
11111	reserved	reserved

TABLE 7-33. Carrier Clock Pulse Width Options

Encoding MCPW Bits 7 6 5	Low Frequency (TXHSC = 0)	High Frequency (TXHSC = 1)
0 0 0	Reserved	Reserved
0 0 1	Reserved	Reserved
0 1 0	6 µsec	0.7 µsec
0 1 1	7 µsec	0.8 µsec
1 0 0	9 µsec	0.9 µsec
1 0 1	10.6 µsec	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

7.20.3 Consumer-IR Configuration Register (RCCFG), Bank 7, Offset 02h

This register control the basic operation of the Consumer-IR mode. After reset, the content of this register is 00h.

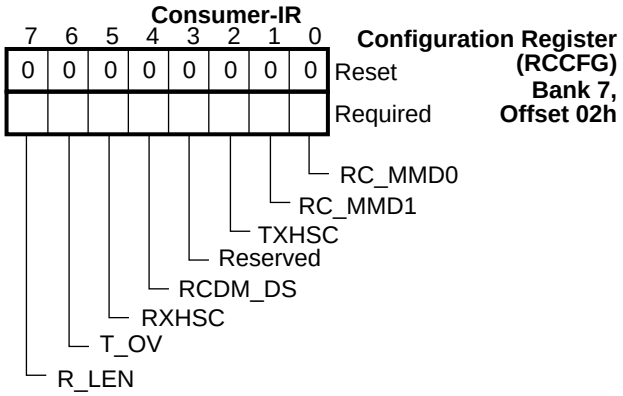


FIGURE 7-51. RCCFG Register Bitmap

Bits 1,0 - Transmitter Modulator Mode (RC_MMD(1,0))

Determines how infrared pulses are generated from the transmitted bit string. (see Table 7-34).

TABLE 7-34. Transmitter Modulation Mode Selection

RCCFG Bits 1 0	Modulation Mode
0 0	**C_PLS Modulation mode.** Pulses are generated continuously for the entire logic 0 bit time.
0 1	**8_PLS Modulation Mode.** 8 pulses are generated each time one or more logic 0 bits are transmitted following a logic 1 bit.
1 0	**6_PLS Modulation Mode.** 6 pulses are generated each time one or more logic 0 bits are transmitted following a logic 1 bit.
1 1	**Reserved.** Result is indeterminate.

Bit 2 - Transmitter Subcarrier Frequency Select (TXHSC)

This bit selects the frequency range for the modulation carrier.

0 - Low frequency: 30-56.9 KHz

1 - High frequency: 400-480 KHz

Bit 3 - Reserved

Read/Write 0.

Bit 4 - Receiver Demodulation Disable (RCDM_DS)

When this bit is 1, the internal demodulator is disabled. The internal demodulator, when enabled, performs carrier frequency checking and envelope detection.

This bit must be set to 1 (disabled), when the demodulation is performed externally, or when oversampling mode is selected to determine the carrier frequency.

0 - Internal demodulation enabled.

1 - Internal demodulation disabled.

Bit 5 - Receiver Carrier Frequency Select (RXHSC)

This bit selects the frequency range for the receiver demodulator.

0 - Low frequency: 30-56.9 KHz

1 - High frequency: 400-480 KHz

Bit 6 - Receiver Sampling Mode Select(T_OV)

0 - Programmed-T-period sampling.

1 - Oversampling mode.

Bit 7 - Run Length Control (R_LEN)

Enables or disables run length encoding/decoding. The format of a run length code is:

YXXXXXXX

where, Y is the bit value and XXXXXXX is the number of bits minus 1 (Selects from 1 to 128 bits).

0 - Run Length Encoding/decoding is disabled.

1 - Run Length Encoding/decoding is enabled.

7.20.4 Link Control/Bank Select Registers (LCR/BSR), Bank 7, Offset 03h

These registers are the same as the registers at offset 03h in bank 0.

7.20.5 Infrared Interface Configuration Register 1 (IRCFG1), Bank 7, Offset 04h

This register holds the transceiver configuration data for Sharp-IR and SIR modes. It is also used to directly control the transceiver operation mode when automatic configuration is not enabled. The four least significant bits are also used to read the identification data of a Plug and Play infrared interface adaptor.

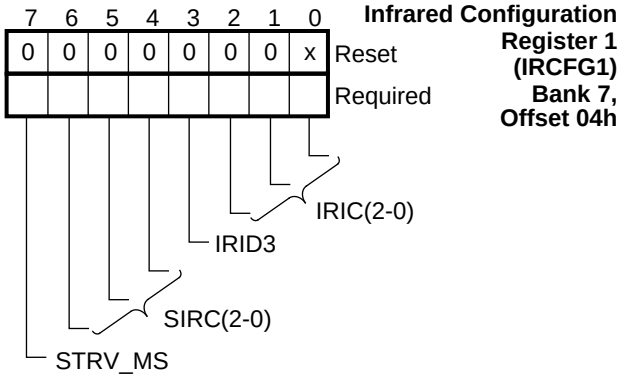


FIGURE 7-52. IRCFG1 Register Bitmap

Bit 0 - Transceiver Identification/Control Bit 0 (IRIC0)

The function of this bit depends on whether the ID0/IRSL0/IRRX2 pin is programmed as an input or an output.

If ID0/IRSL0/IRRX2 is programmed as an input (IRSL0_DS = 0) then:

— Upon read, this bit returns the logic level of the pin (allowing external devices to identify themselves).

— Data written to this bit position is ignored.

If ID0/IRSL0/IRXX2 is programmed as an output (IRSL0_DS = 1), then:

— If AMCFG (bit 7 of IRCFG4) is set to 1, this bit drives the ID0/IRSL0/IRRX2 pin when Sharp-IR mode is selected.

— If AMCFG is 0, this bit will drive the ID0/IRSL0/IRRX2 pin, regardless of the selected mode.

Upon read, this bit returns the value previously written.

Bits 2-1 - Transceiver Identification/Control Bits 2-1 (IRIC2-1)

The function of these bits depends on whether the ID/IRSL(2-1) pins are programmed as inputs or outputs.

If ID/IRSL(2-1) are programmed as input (IRSL21_DS = 0) then:

Upon read, these bits return the logic level of the pins (allowing external devices to identify themselves).

Data written to these bit positions will be ignored.

If ID/IRSL(2-1) are programmed as output (IRSL21_DS = 1) then:

If AMCFG (bit 7 of IRCFG4) is set to 1, these bits drive the ID/IRSL(2-1) pins when Sharp-IR mode is selected.

If AMCFG is 0, these bits will drive the ID/IRSL(2-1)pins, regardless of the selected mode.

Upon read, these bits return the values previously written.

Bit 3 - Transceiver identification (IRID3)

Upon read, this bit returns the logic level of the ID3 pin.

Data written to this bit position is ignored.

Bits 6-4 - SIR Mode Transceiver Configuration (SIRC(2-0))

These bits will drive the ID/IRSL(2-0) pins when AMCFG (bit 7 of IRCFG4) is 1 and SIR mode is selected. They are unused when AMCFG is 0 or when the ID/IRSL (2-0) pins are programmed as inputs. SIRC0 is also unused when the IRSL0_DS bit in IRCFG4 is 0.

Upon read, these bits return the values previously written.

Bit 7 - Special Transceiver Mode Selection (STRV_MS)

This bit supports programming of the high speed mode in some optical devices. When this bit is set to 1, the IRTX output signal is forced to active high and a timer is started.

The timer times out after 64 µsec, at which time the bit is reset and the IRTX output signal becomes low again. The timer is restarted every time a 1 is written to this bit.

Although it is possible to extend the period during which IRTX remains high beyond 64 µsec, this should be avoided to prevent damage to the transmitter LED.

Writing a zero to this bit has no effect.

7.20.6 Infrared Interface Configuration Register 2 (IRCFG2), Bank 7, Offset 05h

IRCFG2 holds the transceiver configuration data for the **MIR** and **FIR** modes.

Upon reset, the content of this register is 00h.

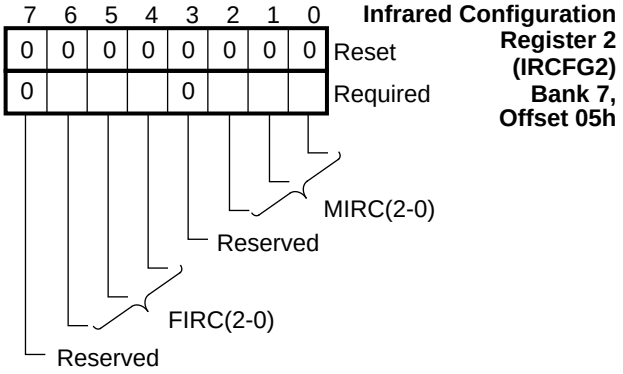


FIGURE 7-53. IRCFG2 Register Bitmap

Bits 2-0 - MIR Mode Transceiver Configuration (MIRC(2-0))

These bits drive the ID/IRSL(2-0) pins when AMCFG (bit 7 of IRCFG4) is 1 and MIR mode is selected. They are unused when AMCFG is 0 or when the ID/IRSL(2-0) pins are programmed as inputs.

Upon read, these bits return the values previously written.

Bit 3 - Reserved

Read/Write 0.

Bits 6-4 - FIR Mode Transceiver Configuration (FIRC(2-0))

These bits drive the IRSL(2-0) pins when AMCFG is 1 and FIR mode is selected. They are unused when AMCFG (bit 7 of IRCFG4) is 0 or when the ID/IRSL(2-0) pins are programmed as inputs. Upon read, these bits return the values previously written.

Bit 7 - Reserved

Read/Write 0.

7.20.7 Infrared Interface Configuration 3 Register (IRCFG3), Bank 7, Offset 06h

This register sets the external transceiver configuration for the low speed and high speed Consumer IR modes of operation. Upon reset, the content of this register is 00h.

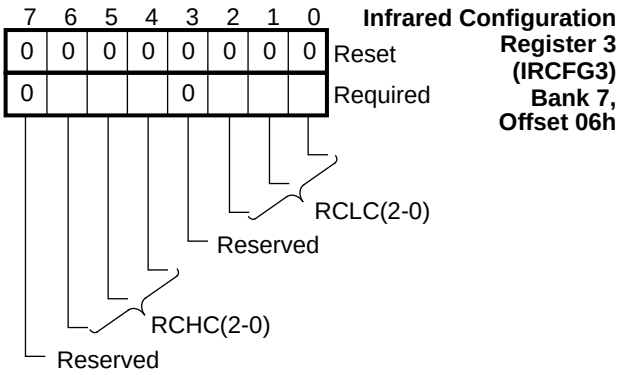


FIGURE 7-54. IRCFG3 Register Bitmap

Bits 2-0 - Consumer-IR Mode Transceiver Configuration, Low-Speed (RCLC)

These bits drive the ID/IRSL(2-0) pins when AMCFG is 1 and Consumer-IR mode with 30-56 KHz receiver carrier frequency is selected. They are unused when AMCFG is 0 or when the ID/IRSL(2-0) pins are programmed as inputs. Upon read, these bits return the values previously written.

Bit 3 - Reserved

Read/Write 0.

Bits 6-4 - Consumer-IR Mode Transceiver Configuration, High-Speed (RCHC)

These bits drive the IRSL(2-0) pins when AMCFG (bit 7 of IRCFG4) is 1 and Consumer-IR mode with 400-480 KHz receiver carrier frequency is selected. They are unused when AMCFG is 0 or when the ID/IRSL(2-0) pins are programmed as inputs.

Upon read, these bits return the values previously written.

Bit 7 - Reserved

Read/Write 0.

7.20.8 Infrared Interface Configuration Register 4 (IRCFG4), Bank 7, Offset 07h

This register configures the receiver data path and enables the automatic selection of the configuration pins.

After reset, this register contains 00h.

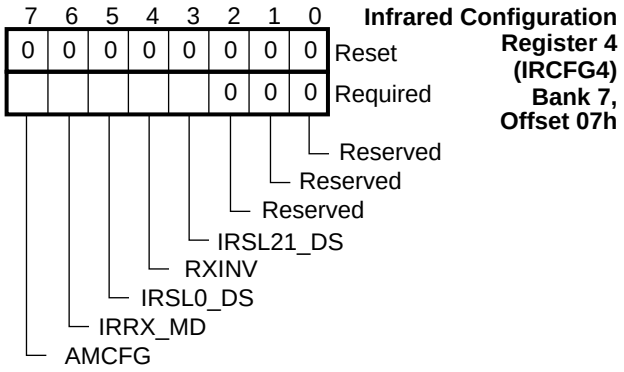


FIGURE 7-55. IRCFG4 Register Bitmap

Bits 2-0 - Reserved

Read/write 0.

Bit 3- ID/IRSL(2-1) Pins' Direction Select (IRSL21_DS)

This bit determines the direction of the ID/IRSL2 and ID/IRSL1 pins.

0 - Pins' direction is input.

1 - Pins' direction is output.

Bit 4 - IRRX Signal Invert (RXINV)

This bit supports optical transceivers with receive signals of opposite polarity (active high instead of active low).

When set to 1 an inverter is put on the path of the input signal of the receiver.

Bit 5 - ID0/IRSL0/IRRX2 Pin Direction Select (IRSL0_DS)

This bit determines the direction of the ID0/IRSL0/IRRX2 pin.

0 - Pin's direction is input.

1 - Pin's direction is output.

Bit 6 - Infrared Mode Selection (IRRX_MD)

Determines whether one or two inputs are used for IrDA low speed and high speed input signals.

Table 7-35 shows the possible combinations of IRSL0_DS, IRRX_MD and AUX_IRRX.

0 - One input pin is used for both low and high-speed IR modes.

1 - Low-speed input is on IRRX1 and High-speed is on IRRX2.

Bit 7 - Automatic Module Configuration (AMCFG)

When set to 1, this bit enables automatic infrared configuration.

TABLE 7-35. Infrared Receiver Input Selection

Bit 5 of IRCFG4[a] (IRSL0_DS)	Bit 6 of IRCFG4[a] (IRRX_MD)	Bit 4 of IRCR2 (AUX_IRRX)[b]	HIS_IR (1 when MIR or FIR selected)	Selected IRRX
0	0	0	x	IRRX1
0	0	1	x	IRRX2
0	1	x	0	IRRX1
0	1	x	1	IRRX2
1	0	0	x	IRRX1
1	0	1	x	1
1	1	x	0	IRRX1
1	1	x	1	1

a. IRCFG4 is in bank 7, offset 07h. It is described on page 148.
b. AUX_IRRX (bit 4 of IRCR2) is described on page 138.

7.21 UART WITH FAST IR REGISTER BITMAPS

Read Cycles

Receiver Data Register (RXD) Bank 0, Offset 00h

7	6	5	4	3	2	1	0	
								Reset
								Required

Received Data

Extended Mode, Read Cycles

Event Identification Register (EIR) Bank 0, Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1	Reset
								Required

RXHDL_EV
TXLDL_EV
LS_EV or TXHLT_EV
MS_EV
DMA_EV
TXEMP-EV or PLD_EV
SFIF_EV (FIR and MIR only)
TMR_EV

Write Cycles

Transmitter Data Register (TXD) Bank 0, Offset 00h

7	6	5	4	3	2	1	0	
								Reset
								Required

Transmitted Data

Write Cycles

FIFO Control Register (FCR) Bank 0, Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
				0				Required

FIFO_EN
RXSR
TXSR
Reserved
TXFTH0
TXFTH1
RXFTH0
RXFTH1

Extended Mode

Interrupt Enable Register (IER) Bank 0, Offset 01h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

RXHDL_IE
TXLDL_IE
LS_IE or TXUR_IE
MS_IE
DMA_IE
TXEMP_IE or PLD_IE
SFIF_IE (MIR and FIR only)
TMR_IE

Link Control Register (LCR) All Banks, Offset 03h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

WLS0
WLS1
STB
PEN
EPS
STKP
SBRK
BKSE

Non-Extended Modes, Read Cycles

Event Identification Register (EIR) Bank 0, Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1	Reset
		0	0					Required

IPF - Interrupt Pending
IPR0 - Interrupt Priority 0
IPR1 - Interrupt Priority 1
RXFT - RX_FIFO Time-Out
Reserved
Reserved
FEN0 - FIFO Enabled
FEN1 - FIFO Enabled

Bank Selection Register (BSR) All Banks, Offset 03h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

Bank Selected

BKSE-Bank Selection Enable

Non-Extended Mode

Modem Control Register (MCR) Bank 0, Offset 04h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0						Required

DTR
RTS
RILP
ISEN or DCDLP
LOOP
Reserved
Reserved
Reserved

Non-Extended Mode

Scratch Register (SCR) Bank 0, Offset 07h

7	6	5	4	3	2	1	0	
								Reset
								Required

Scratch Data

Extended Mode

Modem Control Register (MCR) Bank 0, Offset 04h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

DTR
RTS
DMA_EN
TX_DFR
IR_PLS
MDSL0
MDSL1
MDSL2

Extended UART, SIR or Sharp-IR Mode

Auxiliary Status Register (ASCR) Bank 0, Offset 07h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
				0				Required

RXF_TOUT
EOF_INF
S_EOT
Reserved
LOST_FR or RXWDG
RXBSY or RXACT
TXUR
PLD/CTE

Non-Extended Mode

Link Status Register (LSR) Bank 0, Offset 05h

7	6	5	4	3	2	1	0	
0	1	1	0	0	0	0	0	Reset
								Required

RXDA
OE
PE or BAD_CRC
FE or PHY_ERR
BRK or MAX_LEN
TXRDY
TXEMP
ER_INF or FR_END

Legacy Baud Rate Generator Divisor Low Byte Register (LBGD(L) Bank 1, Offset 00h

7	6	5	4	3	2	1	0	
								Reset
								Required

Least Significant Byte of Baud Rate Generator

Modem Status Register (MSR) Bank 0, Offset 06h

7	6	5	4	3	2	1	0	
X	X	X	X	0	0	0	0	Reset
								Required

DCTS
DDSR
TERI
DDCD
CTS
DSR
RI
DCD

Legacy Baud Rate Generator Divisor High Byte Register (LBGD(H)) Bank 1, Offset 01h

7	6	5	4	3	2	1	0	
								Reset
								Required

Most Significant Byte of Baud Rate Generator

Baud Rate Generator Divisor Low Byte Register (BGD(L)) Bank 2, Offset 00h

7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	Reset
								Required

Least Significant Byte of Baud Rate Generator

IrDA or Consumer-IR Modes

TX_FIFO Current Level Register (TXFLV) Bank 2, Offset 06h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0							Required

TFL0, TFL1, TFL2, TFL3, TFL4, TFL5, Reserved, Reserved

Baud Rate Generator Divisor High Byte Register (BGD(H)) Bank 2, Offset 01h

7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	Reset
								Required

Most Significant Byte of Baud Rate Generator

IrDA or Consumer-IR Modes

RX_FIFO Current Level Register (RXFLV) Bank 2, Offset 07h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0							Required

RFL0, RFL1, RFL2, RFL3, RFL4, RFL5, Reserved, Reserved

Extended Control and and Status Register 1 (EXCR1) Bank 2, Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
	1							Required

EXT_SL, DMANF, DMATH, DMASWP, LOOP, ETDLBK, Reserved, BTEST

Module Revision ID Register (MRID) Bank 3 Offset 00h

7	6	5	4	3	2	1	0	
0	0	1	0	x	x	x	x	Reset
								Required

Revision ID(RID 3-0)

Module ID(MID 7-4)

Extended Control and and Status Register 2 (EXCR2) Bank 2, Offset 04h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
	0							Required

TF_SIZ0, TF_SIZ1, RF_SIZ0, RF_SIZ1, PRESL0, PRESL1, Reserved, LOCK

Shadow of Link Control Register (SH_LCR) Bank 3, Offset 01h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

WLS0, WLS1, STB, PEN, EPS, STKP, SBRK, BKSE

Shadow of FIFO Control Register (SH_FCR) Bank 3, Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
				0				Required

FIFO_EN
RXFR
TXFR
Reserved
TXFTH0
TXFHT1
RXFTH0
RXFTH1

Transmission Frame Length or Current Count Least Significant Bits (TFRL(L) or TFRCC(L)) Register Bank 4, Offset 04h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

Least Significant Bits of Transmission Frame Length or Current Count

Interval Timer Low Byte Register (TMR(L)) Bank 4, Offset 00h

7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	Reset
								Required

Least Significant Bits of Interval Timer

Transmission Frame Length or Current Count Most Significant Bits (TFRL(H) or TFRCC(H)) Register Bank 4, Offset 05h

7	6	5	4	3	2	1	0	
0	0	0	0	1	0	0	0	Reset
0	0	0						Required

Most Significant Bits of Transmission Frame Length or Current Count

Always 0

Interval Timer High Byte Register (TMR(H)) Bank 4, Offset 01h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	0					Required

Most Significant Bits of Interval Timer

Reserved

Reception Frame Maximum Length LSB or Current Count LSB (RFRML(L) or RFRCC(L)) Register Bank 4, Offset 06h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

Least Significant Bits of Reception Frame Length or Current Count

Infrared Control Register1 (IRCR1) Bank 4, Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	0					Required

TMR_EN
CTEST
IR_SL0
IR_SL1

Reserved

Reception Frame Maximum Length MSB or Current Count MSB (RFRML(H) or RFRCC(H)) Register Bank 4, Offset 07h

7	6	5	4	3	2	1	0	
0	0	0	0	1	0	0	0	Reset
0	0	0						Required

Most Significant Bits of Reception Frame Length or Current Count

Always 0

Pipeline Baud Rate Generator Divisor Low and High Byte (P_BGD(L) and P_BGD(H)) Bank 5, Offsets 00h,01h

7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	Reset
								Required

High/Low Divisor Byte

Reception Frame Length FIFO Bottom LSB Register (RFRL(L)) or Lost Frame Count LSB Register (LSTFRC) Bank 5, Offset 06h

7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	Reset
								Required

Least Significant Bits of Received Frame Length FIFO Bottom or of the Lost Frame Count

Pipeline Mode Register (P_MDR) Bank 5, Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
								Required

MD_PEN
BR_PEN
P_DMA_EN
P_DMASWP
Reserved
P_MDSL0
P_MDSL1
P_MDSL2

Reception Frame Length FIFO Bottom MSB Register (RFRL(H)) Bank 5, Offset 07h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0						Required

Least Significant Bits of Received Frame Length FIFO Bottom or of the Lost Frame Count

Reserved

Infrared Control Register 2 (IRCR2) Bank 5, Offset 04h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	0	Reset
0								Required

IR_FDPLX
IRMSSL
MDRS
TX_MS
AUX_IRRX
FEND_MD
SFTSL
Reserved

Infrared Control Register 3 (IRCR3) Bank 6, Offset 00h

7	6	5	4	3	2	1	0	
0	0	1	0	0	0	0	0	Reset
				0			0	Required

Reserved
TXCRC_DS
TXCRC_INV
Reserved
MIR_CRC
FIR_CRC
SHMD_DS
SHDM_DS

Frame Status FIFO Bottom Register (FRM_ST) Bank 5, Offset 05h

7	6	5	4	3	2	1	0	
0	0	x	0	0	0	0	0	Reset
								Required

OVR2
OVR1
BAD_CRC
PHY_ERR
MAXLEN
Reserved
LOST_FR
VLD

MIR Pulse Width Register (MIR_PW) Bank 6, Offset 01h

7	6	5	4	3	2	1	0	
0	0	0	0	1	0	1	0	Reset
0	0	0	0					Required

MPW(3-0)

Reserved

SIR Pulse Width Register (SIR_PW) Bank 6, Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	0					Required

SPW(3-0)

Reserved

Consumer-IR Mode

Configuration Register (RCCFG) Bank 7, Offset 02h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
				0				Required

RC_MMD0

RC_MMD1

TXHSC

Reserved

RCDM_DS

RXHSC

T_OV

R_LEN

Beginning Flags and Preamble Length Register (BFPL) Bank 6, Offset 04h

7	6	5	4	3	2	1	0	
0	0	1	0	1	0	1	0	Reset
								Required

FPL(3-0)

MBF(7-4)

Infrared Configuration Register 1 (IRCFG1) Bank 7, Offset 04h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	x	Reset
								Required

IRIC(2-0)

IRID3

SIRC(2-0)

STRV_MS

Infrared Receiver Demodulation Control Register (IRRXDC) Bank 7, Offset 00h

7	6	5	4	3	2	1	0	
0	0	1	0	1	0	0	1	Reset
								Required

DFR0

DFR1

DFR2

DFR3

DFR4

DBW0

DBW1

DBW2

Infrared Configuration Register 2 (IRCFG2) Bank 7, Offset 05h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0				0				Required

MIRC(2-0)

Reserved

FIRC(2-0)

Reserved

Infrared Transmitter Modulation Control Register (IRTXMC) Bank 7, Offset 01h

7	6	5	4	3	2	1	0	
0	1	1	0	1	0	0	1	Reset
								Required

MCFR(4-0)

MCPW(2-0)

Infrared Configuration Register 3 (IRCFG3) Bank 7, Offset 06h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0				0				Required

RCLC(2-0)

Reserved

RCHC(2-0)

Reserved

Infrared Configuration Register 4 (IRCFG4) Bank 7, Offset 07h

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
					0	0	0	Required

Reserved

IRSL21_DS

RXINV

IRSL0_DS

IRRX_MD

AMCFG

8.0 General Purpose Input and Output (GPIO) Ports (Logical Device 7) and Chip Select Output Signals

8.1 GENERAL PURPOSE INPUT AND OUTPUT (GPIO) PORTS

The PC87308VUL supports two identical General Purpose I/O (GPIO) ports.

Activation and deactivation (enable/disable) of GPIO ports is controlled by the Activate register (index 30h) of logical device 7 and by bit 7 of the Function Enable Register 2 (FER2) of the Power Management logical device. See Section 9.2.4 on page 159.

The base address of the GPIO ports is software configurable. It is controlled by two base address registers at indexes 60h and 61h of logical device 7. See Table 2-19 on page 20.

The registers that control the GPIO ports are in two banks. The active bank is selected by the GPIO Bank Select bit, bit 7 of SuperI/O Configuration 2 register, at index 22h.

Five registers control GPIO Port 1 and four registers control GPIO Port 2. The registers that control Port 1 are at offsets 00h through 03h from the base address in bank 0 and at offset 00h in bank 1. The registers that control Port 2 are at offsets 04h through 07h from the base address in bank 0. See Tables 8-1 and 8-2.

- Port Data registers at offsets 00h and 04h read or write the data bits of Ports 1 and 2, respectively.
- Port Direction registers at offsets 01h and 05h control the direction of each bit of Ports 1 and 2, respectively.
- Port Output Type registers at offsets 02h and 06h control the buffer type (open-drain or push-pull) of each bit of Ports 1 and 2, respectively.
- The GPIO ports have open-drain output signals with internal pull-ups and TTL input signals. Pull-up Control registers at offsets 03h and 07h enable or disable the internal pull-up capability of each bit of Ports 1 and 2, respectively.

Note that GPIO21 on pin 77 is unaffected by the output type or direction registers - it is always push-pull with no internal pullup.

The output type and pull-up settings for the GPIO17,16 signals can be locked by setting bits 7,6 of the Port 1 Lock register in bank 1.

Reading an output pin returns the internally latched bit value, not the pin value.

Writing to an input pin has no effect on the pin, except for internally latching the written value. The latched value is reflected on the pin when the direction changes to output. Upon reset the write latches are initialized to FFh.

The port pins are back-drive protected when the PC87308VUL is powered down and also when the port is inactive (disabled). AC and DC are the same as the $\overline{STB}$ pin, except for I_{OH}/I_{OL} of 4 mA.

The GPIO signals are multiplexed as follows:

- GPIO27-24 are multiplexed with the X-Bus Data Buffer (XDB) signals XD5-2, respectively.
- GPIO23 is multiplexed with $\overline{RING}$.
- GPIO22 is multiplexed with $\overline{POR}$.
- GPIO21 is multiplexed with IRSL0 and IRSL2.
- GPIO20 is multiplexed with IRSL1.

A GPIO port must not be enabled at the same address as another accessible PC87308VUL register. Undefined results will occur if a GPIO is configured in this way.

TABLE 8-1. The GPIO Registers, Bank 0

GPIO Register	Offset	Type	Hard Reset Value	Detailed Description
Port 1 Data	00h	R/W	FFh	Reads return the bit or pin value, according to the direction bit. Writes are saved in this register and affect the output pins.
Port 1 Direction	01h	R/W	00h	Each bit controls the direction of the corresponding port pin. 0 - Input. Reads of Port Data register return pin value. 1 - Output. Reads of Port Data register return bit value.
Port 1 Output Type	02h	R/W	00h	Each bit controls the type of the corresponding port pin. 0 - Open-drain. 1 - Push-pull.
Port 1 Pull-up Control	03h	R/W	FFh	Each bit controls the internal pull-up for the corresponding port pin. 0 - No internal pull-up. 1 - Internal pull-up.
Port 2 Data	04h	R/W	FFh	Same as Port 1 Data register.
Port 2 Direction	05h	R/W	00h	Same as Port 1 Direction register.
Port 2 Output Type	06h	R/W	00h	Same as Port 1 Output Type register.
Port 2 Pull-up Control	07h	R/W	FFh	Same as Port 1 Pull-up Control register.

TABLE 8-2. The GPIO Registers, Bank 1

GPIO Register	Offset	Type	Hard Reset Value	Detailed Description
Port 1 Lock Register	00h	R/W	00h	Bits 5-0 are reserved. Bits 7,6 lock the Port 1 control settings for bits GPIO17,16, respectively. Setting them to 1 locks the corresponding output type and pull-up bit settings. Only master reset unlocks these bits by setting them to 0s.
Reserved	01h-07h	-	-	-

8.2 PROGRAMMABLE CHIP SELECT OUTPUT SIGNALS

The PC87308VUL has three programmable chip select signals: $\overline{CS}$2-0. $\overline{CS0}$ is an open drain output signal ($\overline{CS1}$ and $\overline{CS2}$ have push-pull buffers). $\overline{CS0}$ is in TRI-STATE when no V_{DD} is applied.

Activation and deactivation (enabling and disabling) of these chip select signals are controlled by the Function Enable Register 2 (FER2) of logical device 8 (see section 9.2.4 on page 159) and the configuration registers for $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$ at second level indexes 02h, 06h and 0Ah, respectively.

These registers are accessed using two index levels.

The first level index points to the Programmable Chip Select Index and Data registers, like other PC87308VUL configuration registers. See Sections 2.4.3 and 2.4.4 on page 22. The Programmable Chip Select Configuration Index and Data registers are at index 23h and 24h respectively.

The second level points to one of the three registers for each $\overline{CS}$ pin. See “Programmable Chip Select Configuration Registers” on page 25. Each $\overline{CS}$ pin is configured by the three registers assigned to it. One specifies the base address MSB. One specifies the base address LSB and one configures the $\overline{CS}$ pin.

All 16 address bits are decoded, with five mask options to ignore (not decode) address bits A0, A1, A2, A3 and A4-11. Decoding of only address and AEN pins, without $\overline{RD}$ or $\overline{WR}$ pins, is also supported.

A $\overline{CS}$ signal is asserted when an address match occurs and may be qualified by $\overline{RD}$ or $\overline{WR}$ signal(s). An address match occurs when the AEN signal is inactive (low) and the non-masked address pins match the corresponding base address bits.

9.0 Power Management (Logical Device 8)

9.1 FUNCTIONAL OVERVIEW

The power management logical device provides the system user with hardware configuration options. Registers in this logical device enable chip device functions, and set I/O characteristics for certain pins.

9.2 THE POWER MANAGEMENT REGISTERS

The power management registers are accessed via the Power Management Index and Data registers, which are located at base address and base address + 01h, respectively. The base address is indicated by the Base Address registers at indexes 60h and 61h of logical device 8, respectively. See Table 2-20 on page 21.

Table 9-1 lists the power management registers.

TABLE 9-1. The Power Management Registers

Index	Symbol	Description	Type
Base + 00h		Power Management Index Register	R/W
Base + 01h		Power Management Data Register	R/W
00h	FER1	Function Enable Register 1	R/W
01h	FER2	Function Enable Register 2	R/W
02h	PMC1	Power Management Control 1	R/W
03h	PMC2	Power Management Control 2	R/W
04h	PMC3	Power Management Control 3	R/W

9.2.1 Power Management Index Register, Base Address + 00h

This read/write register is reset by hardware to 00h. It points to one of the power management registers. Bits 7 through 3 are read only and return 00000 when read. See Figure 9-1.

The data in the indicated register is accessed via the Power Management Data register at the base address + 01h.

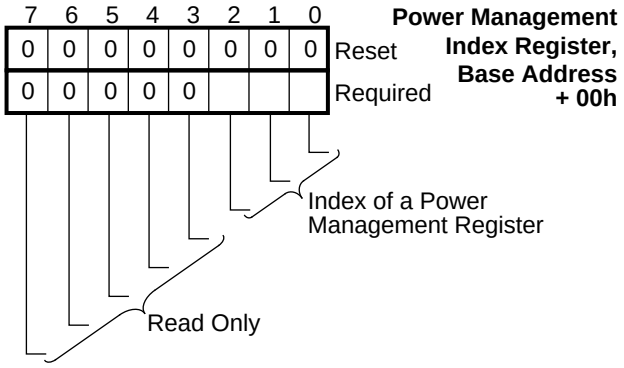


FIGURE 9-1. Power Management Index Register Bitmap

9.2.2 Power Management Data Register, Base Address + 01h

This read/write register contains the data in the register pointed to by the Power Management Index register at the base address. See Figure 9-2.

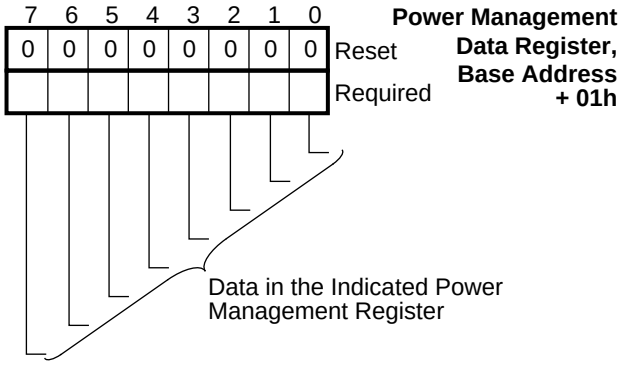


FIGURE 9-2. Power Management Data Register Bitmap

9.2.3 Function Enable Register 1 (FER1), Index 00h

Hardware resets this read/write register to FFh.

A set bit enables activation of the corresponding logical device via its Active register at index 30h.

A cleared bit disables the corresponding logical device regardless of the value in its Active register. Bit 0 of the Active register of a logical device is ignored when the corresponding FER1 bit is cleared. See Figure 9-3.

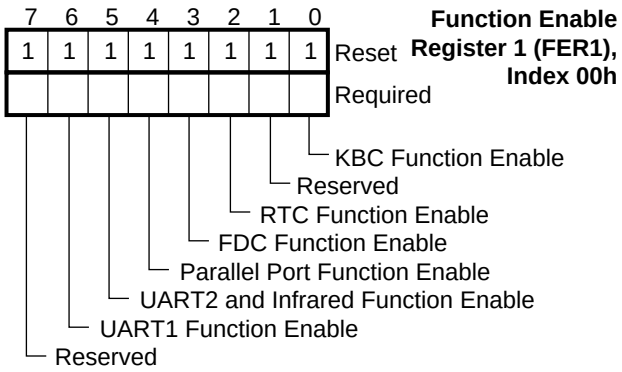


FIGURE 9-3. Function Enable Register 1 Bitmap

Bit 0 - KBC Function Enable

0 - Disabled.

1 - Enabled. (Default)

Bit 1 - Reserved

Reserved.

Bit 2 - RTC Function Enable

0 - Disabled.

1 - Enabled. (Default)

Bit 3 - FDC Function Enable

0 - Disabled.

1 - Enabled. (Default)

Bit 4 - Parallel Port Function Enable

0 - Disabled. (Default).

1 - Enabled.

Bit 5 - UART2 and Infrared Function Enable

0 - Disabled. (Default).

1 - Enabled.

Bit 6 - UART1 Function Enable

0 - Disabled. (Default).

1 - Enabled.)

Bit 7 - Reserved

Reserved.

9.2.4 Function Enable Register 2 (FER2), Index 01h

Hardware resets this read/write register to FFh.

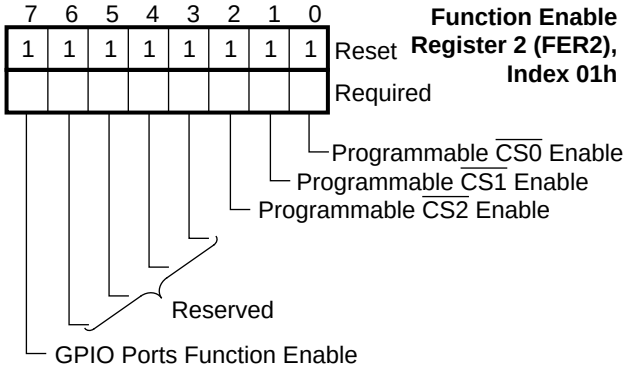


FIGURE 9-4. FER2 Register Bitmap

Bit 0 - Programmable $\overline{\text{CS0}}$ Function Enable

See $\overline{\text{CS0}}$ Configuration 0 register in Section 2.10.3 on page 25.

0 - $\overline{\text{CS0}}$ is disabled. $\overline{\text{CS0}}$ pin is not asserted, $\overline{\text{CS0}}$ configuration and base address registers are maintained.

1 - $\overline{\text{CS0}}$ is enabled. (Default)

Bit 1 - Programmable $\overline{\text{CS1}}$ Function Enable

See $\overline{\text{CS1}}$ Configuration 1 register in Section 2.10.7 on page 26.

0 - $\overline{\text{CS1}}$ is disabled. $\overline{\text{CS1}}$ signal is not asserted, $\overline{\text{CS1}}$ Configuration and base address registers are maintained.

1 - $\overline{\text{CS1}}$ is enabled. (Default)

Bit 2 - Programmable $\overline{\text{CS2}}$ Function Enable

See $\overline{\text{CS2}}$ Configuration 2 register in Section 2.10.11 on page 27.

0 - $\overline{\text{CS2}}$ is disabled. The $\overline{\text{CS2}}$ signal is not asserted, $\overline{\text{CS2}}$ Configuration and base address registers are maintained.

1 - $\overline{\text{CS2}}$ is enabled. (Default)

Bits 6-3 - Reserved

Reserved.

Bit 7 - GPIO Ports Function Enable

0 - GPIO Ports 1 and 2 are inactive (disabled). Reads and writes are ignored; registers and pins are maintained. Bit 0 of the Activate register (index 30h) of the GPIO Ports logical device is ignored. (Default)

1 - GPIO Ports 1 and 2 are active (enabled) when bit 0 of the Activate register (index 30h) of the GPIO Ports logical device is set.

9.2.5 Power Management Control 1 (PMC1), Index 02h

Hardware resets this read/write register to 00h.

A set bit puts the signals of the corresponding inactive logical device in TRI-STATE (except IRQ and DMA pins) regardless of the value of bit 0 of the corresponding logical device register at index F0h.

A cleared bit has no effect. In this case, the TRI-STATE status of signals is controlled by bit 0 of the corresponding logical device register at index F0h.

This is an OR function between PMC1 and the register at index F0h of the corresponding logical device.

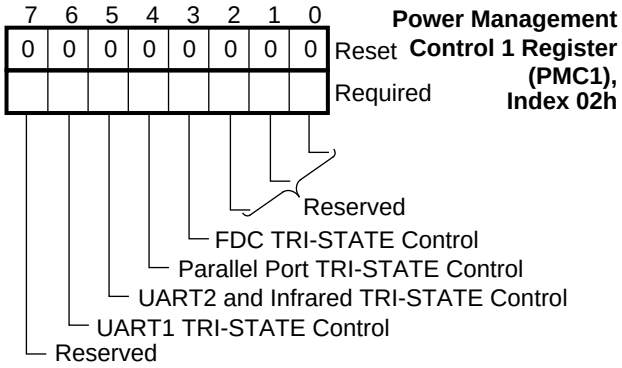


FIGURE 9-5. PMC1 Register Bitmap

Bits 2-0 - Reserved

These bits are reserved.

Bit 3 - FDC TRI-STATE Control

0 - No effect. TRI-STATE controlled by bit 0 of the SuperI/O FDC Configuration register. (Default)

See Section 2.6.1 on page 23.

1 -FDC signals are in TRI-STATE.

Bit 4 - Parallel Port TRI-STATE Control

0 - No effect. TRI-STATE controlled by bit 0 of the SuperI/O Parallel Port Configuration register. (Default)

See Section 2.7.1 on page 24.

1 - Parallel Port signals are in TRI-STATE.

Bit 5 - UART2 and Infrared TRI-STATE Control

0 - No effect. TRI-STATE controlled by bit 0 of the SuperI/O UART2 Configuration register. (Default)

See Section 2.8.1 on page 24.

1 - UART2 signals are in TRI-STATE.

Bit 6 - UART1 TRI-STATE Control

0 - No effect. TRI-STATE controlled by bit 0 of the SuperI/O UART1 Configuration register. (Default)

See Section 2.9.1 on page 25.

1 - UART1 signals are in TRI-STATE.

Bit 7 - Reserved

Reserved.

9.2.6 Power Management Control 2 Register (PMC2), Index 03h

Hardware resets this read/write register according to the CFG2 and CFG3 strap pins, the status of the multiplier clock and the hardware configuration. See “Hardware Configuration” on page 11 and the description of the bits in this register.

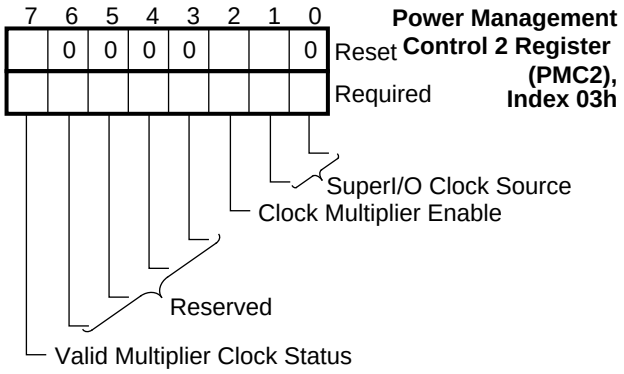


FIGURE 9-6. PMC2 Register Bitmap

Bits 1,0 - Super/O Clock Source

Bit 0 is the Least Significant Bit (LSB).

00 - The 24 MHz clock is fed via the X1 pin.

01 - Reserved.

10 - The 48 MHz clock is fed via the X1 pin.

11 - The clock source is the on-chip clock multiplier.

Bit 2 - Clock Multiplier Enable

0 - On-chip clock multiplier is disabled.

1 - On-chip clock multiplier is enabled.

Bits 6-3 - Reserved

These bits are reserved.

Bit 7 - Valid Multiplier Clock Status

This bit is read only.

0 - On-chip clock (clock multiplier output) is frozen.

1 - On-chip clock (clock multiplier output) is stable and toggling.

9.2.7 Power Management Control 3 Register (PMC3), Index 04h

Hardware resets this register to 0Eh.

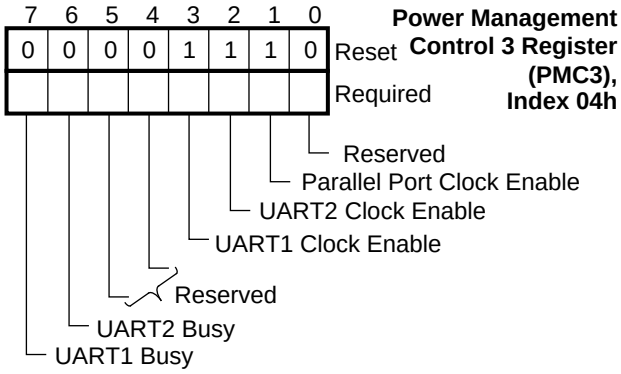


FIGURE 9-7. PMC3 Register Bitmap

Bit 0 - Reserved

This bit is reserved.

Bit 1 - Parallel Port Clock Enable

This bit is ANDed with bit 1 of the SuperI/O Parallel Port Configuration register at index F0h of logical device 4. If either bit is cleared to 0, the clock is disabled. Both bits must be set to 1 to enable the clock.

0 - The clock is disabled.

1 - If bit 1 of the SuperI/O Parallel Port Configuration register is set to 1, the clock is enabled. (Default)

Bit 2 - UART 2 Clock Enable

This bit is ANDed with bit 1 of the SuperI/O UART2 Configuration register at index F0h of logical device 5. If either bit is cleared to 0, the clock is disabled. Both bits must be set to 1 to enable the clock.

0 - The clock is disabled.

1 - If bit 1 of the SuperI/O UART2 Configuration register is set to 1, the clock is enabled. (Default)

Bit 3 - UART 1 Clock Enable

This bit is ANDed with bit 1 of the SuperI/O UART1 Configuration register at index F0h of logical device 6. If either bit is cleared to 0, the clock is disabled. Both bits must be set to 1 to enable the clock.

0 - The clock is disabled.

1 - If bit 1 of the SuperI/O UART1 Configuration register is set to 1, the clock is enabled. (Default)

Bits 5,4 - Reserved

These bits are reserved.

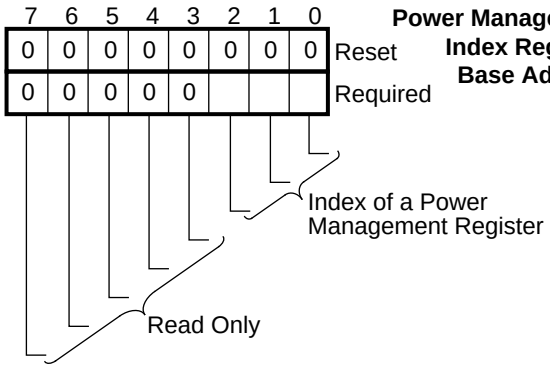
Bit 6 - UART2 Busy

When set to 1, this read-only bit indicates UART2 is busy. It is also accessed via the SuperI/O UART2 Configuration register at index F0h of logical device 5. See Section 2.8 on page 24.

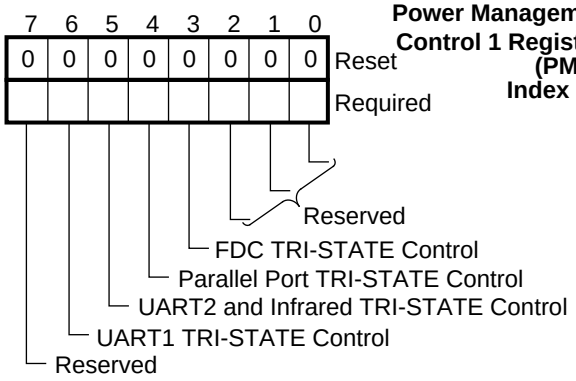
Bit 7 - UART1 Busy

When set to 1, this read-only bit indicates UART1 is busy. It is also accessed via the SuperI/O UART1 Configuration register at index F0h of logical device 6. See Section 2.9 on page 25.

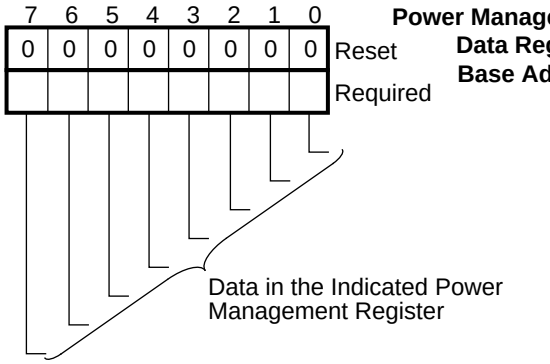
9.3 POWER MANAGEMENT REGISTER BITMAPS



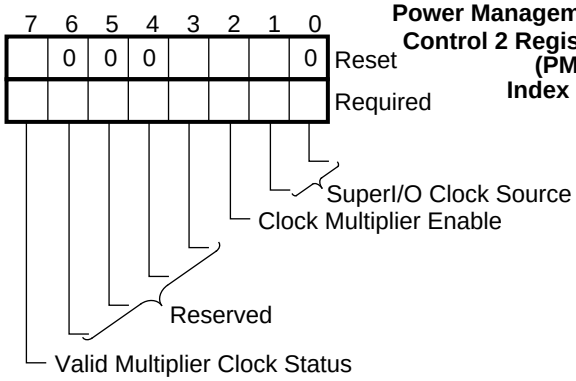
Power Management Index Register, Base Address + 00h



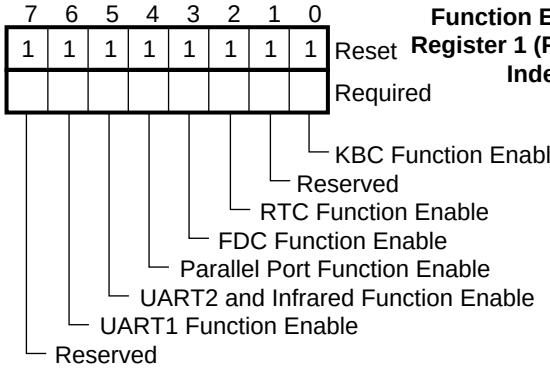
Power Management Control 1 Register, (PMC1) Index 02h



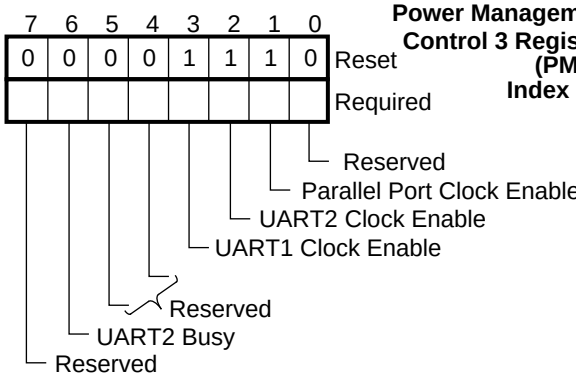
Power Management Data Register, Base Address + 01h



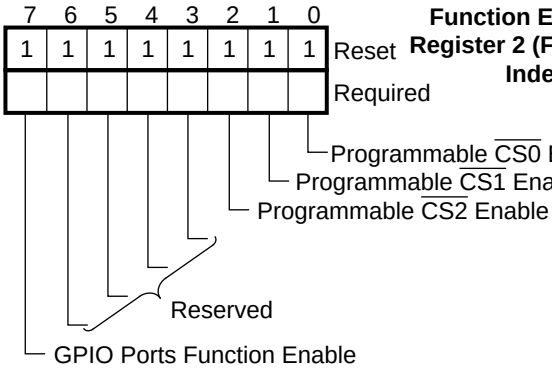
Power Management Control 2 Register (PMC2) Index 03h



Function Enable Register 1 (FER1), Index 00h



Power Management Control 3 Register (PMC3) Index 04h



Function Enable Register 2 (FER2), Index 01h

10.0 X-Bus Data Buffer

10.1 FUNCTIONAL OVERVIEW

The X-Bus Data Buffer (XDB) connects the 8-bit X data bus to the system data bus via the data bus of the PC87308VUL.

The XDB is selected by bit 4 of SuperI/O Chip Configuration 1 register (index 21h), as described in Section 2.4.1 on page 21. This bit is initialized according to the CFG1 strap pin value.

10.2 MAPPING

When XDB is not selected, these pins have alternate functions. See the XDB pin multiplexing Table 1-2 on page 10.

When $\overline{\text{XDCS}}$ is inactive, XD0-7 are neither driven nor gated to D7-0.

When $\overline{\text{XDCS}}$ is active, XD7-0 are linked to D7-0 as follows:

- D7-0 values are driven onto XD7-0 pins when $\overline{\text{XDRD}}$ is inactive
- XD7-0 values are driven onto D7-0 pins when $\overline{\text{XDRD}}$ is active.

11.0 The Internal Clock

11.1 THE CLOCK SOURCE

The source of the internal clock of the PC87308VUL can be 24 MHz or 48 MHz clock signals via the X1 pin, or an internal on-chip clock multiplier fed by the 32.768 KHz crystal of the Real-Time Clock (RTC). The clock source is determined by bits 1,0 of the Power Management Control 2 (PMC2) register of logical device 8. See Section 9.2.6 on page 160. These bits are initialized by the CFG2 and CFG3 strap pins.

Toggling of the 32.768 KHz clock cannot be stopped while V_{CCH} is active. When the 32.768 KHz oscillator is not running, the internal circuit is blocked.

The internal on-chip clock multiplier generates 48 MHz for UART2, and 24 MHz for UART1 and the parallel port.

The Keyboard Controller (KBC) can operate at 8, 12 or 16 MHz. Selection of 8, 12 or 16 MHz for the KBC is done via the SuperI/O KBC Configuration register at index F0h of logical device 0. See Section 2.5.1 on page 23. 16 MHz is not supported when the clock source is 24 MHz via the X1 pin. The KBC clock source can be changed only when the KBC is inactive (disabled).

11.2 THE INTERNAL ON-CHIP CLOCK MULTIPLIER

Two events can trigger the internal on-chip clock multiplier. One is power-on while V_{DD} is active. The other is changing the multiplier enable bit (bit 2 of the PMC2 register of logical device 8) from 0 to 1. See Section 9.2.6 on page 160. This bit can also disable the clock multiplier and its output clock.

Once enabled, the output clock of the clock multiplier is frozen until the clock multiplier can provide an output clock that meets all requirements; then it starts. When the power is turned on, the PC87308VUL wakes up with the internal on-chip clock multiplier enabled, provided that it is selected by the CFG2,3 strap pins.

The 32.768 KHz and output clocks of the internal on-chip clock multiplier operate regardless of the status of the Master Reset (MR) signal. They can operate while MR is active.

The multiplier must have a 32.768 KHz input clock operating. Otherwise, the multiplier waits until this input clock starts operating.

Bit 7 of the PMC2 register of logical device 8 is the Valid Multiplier Clock status bit. When the 32.768 KHz clock toggles before MR becomes active, this bit is usually set to 1 before power-up reset ends (while MR is high, if MR is high for a few msec).

While it is stabilizing, the output clock is frozen and the status bit is cleared to 0 to indicate a frozen clock. When the clock multiplier becomes stable, the output clock starts toggling and the status bit is set to 1. A longer time is required to set the Valid Multiplier Clock status bit if the multiplier waits for a stable 32.768 KHz clock.

The Valid Multiplier Clock status bit indicates when the clock is operating. Software should poll this bit and activate (enable) the KBC, FDC, UART1, the UART2 and infrared interface (IR), and the Parallel Port according to the its value.

The multiplier and its output clock do not use power when they are disabled.

11.3 SPECIFICATIONS

- Wake-up time (from the time V_{DD} becomes valid and the 32.768 KHz clock is operating until the clock becomes stable) is a maximum of 1.5 msec.
- Tolerance (long term deviation) of the multiplier output clock, above the 32.768 KHz tolerance is ± 110 ppm.

  Total tolerance is therefore ± (32.768 KHz clock tolerance + 110 ppm).
- Cycle by cycle variance is a maximum of 0.1 ns.
- Power consumption is a maximum of 5 mA.

12.0 Interrupt and DMA Mapping

The standard Plug and Play Configuration registers map IRQs and DMA channels for the PC87308VUL. See Tables 2-8 and 2-9 starting on page 16.

12.1 IRQ MAPPING

The PC87308VUL allows connection of some logical devices to the 13 IRQ signals.

The polarity of an IRQ signal is controlled by bit 1 of the Interrupt Type registers (index 71h) of each logical device. The same bit also controls selection of push-pull or open-drain IRQ output. High polarity implies push-pull output. Low polarity implies open-drain output with strong pull-up for a short time, followed by weak pull-up.

The IRQ input signals of the KBC or mouse, and of the parallel port are not affected by this bit, i.e., bit 1 at index 71h of each logical device. This bit affects only the output buffer, not the input buffer.

Only UART1 and UART2 may map more than one logical device to any IRQ signal. Other devices may not do so.

An IRQ signal is in TRI-STATE when any of the following conditions is true:

- No logical device is mapped to the IRQ signal.
- The logical device mapped to the IRQ signal is inactive.
- The logical device mapped to the IRQ signal floats its IRQ signal.

12.2 DMA MAPPING

Although the PC87308VUL allows some logical devices to be connected to the four 8-bit DMA channels, it is illegal to map two logical devices to the same pair of DMA signals.

A DRQ signal is in TRI-STATE and the $\overline{\text{DACK}}$ input signal is blocked to 1 when any of the following conditions is true:

- No logical device is mapped to the DMA channel.
- The logical device mapped to the DMA channel is inactive.
- The logical device mapped to the DMA channel floats its DRQ signal.

13.0 Device Description

13.1 GENERAL DC ELECTRICAL CHARACTERISTICS

13.1.1 Recommended Operating Conditions

TABLE 13-1. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{BAT}	Battery Backup Supply Voltage		2.4	3.0	3.7	V
T_A	Operating Temperature		0		+70	°C

13.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur.

Unless otherwise specified, all voltages are relative to ground.

TABLE 13-2. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	6.5	V
V_I	Input Voltage		–0.5	V_{DD} + 0.5	V
V_O	Output Voltage		–0.5	V_{DD} + 0.5	V
T_{STG}	Storage Temperature		–65	+165	°C
P_D	Power Dissipation			1	W
T_L	Lead Temperature Soldering (10 sec.)			+260	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 KΩ [a]	1500		V

a. Value based on test complying with RAI-5-048-RA human body model ESD testing.

13.1.3 Capacitance

TABLE 13-3. Capacitance: T_A = 25°C, f = 1 MHz

Symbol	Parameter	Min	Typical	Max	Unit
C_{IN}	Input Pin Capacitance		5	7	pF
C_{IN1}	Clock Input Capacitance		8	10	pF
C_{IO}	I/O Pin Capacitance		10	12	pF
C_O	Output Pin Capacitance		6	8	pF

13.1.4 Power Consumption Under Recommended Operating Conditions

TABLE 13-4. Power Consumption

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
I_{CC}	V_{DD} Average Main Supply Current [a]	V_{IL} = 0.5 V V_{IH} = 2.4 V No Load		32	50	mA
I_{CCSB}	V_{DD} Quiescent Main Supply Current in Low Power Mode	$V_{IL} = V_{SS}$ $V_{IH} = V_{DD}$ No Load		1.3	1.7	mA
I_{CCH}	V_{CCH} RTC/APC (Logical Device 2) Help Supply Current	V_{CCH} = 5 V ±10%		2		mA
I_{BAT}	V_{BAT} Battery Supply Current.	V_{BAT} = 3 V			2	µA

a. Do not permit V_{CCH} to ramp down at a rate exceeding 1 V/msec. If it does, it may reset the Valid RAM and Time (VRT) bit (bit 7) of the RTC Control Register D (CRD) at offset 0Dh of logical device 2.

13.2 DC CHARACTERISTICS OF PINS, BY GROUP

The following tables list the DC characteristics of all device pins described in Section 1.2. The pin list preceeding each table lists the device pins to which the table applies.

13.2.1 Group 1

Pin List:

A15-0, AEN, $\overline{\text{CTS}}$2,1, $\overline{\text{DACK}}$3-0, $\overline{\text{DCD}}$2,1, $\overline{\text{DSKCHG}}$, $\overline{\text{DSR}}$2,1, $\overline{\text{INDEX}}$, MR, IRRX2,1, $\overline{\text{RD}}$, $\overline{\text{RDATA}}$, SIN2,1, TC, $\overline{\text{TRK0}}$, $\overline{\text{WP}}$, $\overline{\text{WR}}$, $\overline{\text{XDRD}}$

TABLE 13-5. DC Characteristics of Group 1 Pins

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{IH}	Input High Voltage		2.0		V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]		0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$			10	µA
		$V_{IN} = V_{SS}$			–10	µA
V_H	Input Hysteresis		250			mV

a. Not tested. Guaranteed by design.

13.2.2 Group 2

Pin List:

BUSY, PE, SLCT, $\overline{\text{WAIT}}$

Output from SLCT, PE and BUSY is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. (See Table 6-1 on page 85.) Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.

All group 2 pins are back-drive protected.

TABLE 13-6. DC Characteristics of Group 2 Pins

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{IH}	Input High Voltage		2.0		V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]		0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$			100	µA
		$V_{IN} = V_{SS}$			–10	µA

a. Not tested. Guaranteed by design.

13.2.3 Group 3

Pin List:

$\overline{\text{ACK}}$, $\overline{\text{ERR}}$

Output from $\overline{\text{ACK}}$ and $\overline{\text{ERR}}$ is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. (See Table 6-1 on page 85.) Otherwise, output from these signals is level 2.External 4.7 KΩ pull-up resistors should be used.

All group 3 pins are back-drive protected.

TABLE 13-7. DC Characteristics of Group 3 Pins

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{IH}	Input High Voltage		2.0		V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]		0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$			10	µA
		$V_{IN} = V_{SS}$			–100	µA

a. Not tested. Guaranteed by design.

13.2.4 Group 4

Pin List:

MSEN1,0, SELCS

SELCS is a CMOS input pin.

TABLE 13-8. DC Characteristics of Group 4 Pins

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{IH}	Input High Voltage		2.0		V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]		0.8	V
I_{IL}	Input Leakage Current	During Reset: $V_{IN} = V_{DD}$			10	µA
		$V_{IN} = V_{SS}$			–150	µA

a. Not tested. Guaranteed by design.

13.2.5 Group 5

Pin List:

BADDR1,0, CFG3-0

These are CMOS input pins.

TABLE 13-9. DC Characteristics of Group 5 Pins

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{IH}	Input High Voltage		2.5		V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]		1.6	V
I_{IL}	Input Leakage Current	During Reset: $V_{IN} = V_{DD}$			150	µA
		$V_{IN} = V_{SS}$			–10	µA

a. Not tested. Guaranteed by design.

13.2.6 Group 6

Pin List:

X1

TABLE 13-10. DC Characteristics of Group 6 Pins

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{IH}	Input High Voltage		2.0		V_{DD} [a]	V
V_{IL}	Input Low Voltage		-0.5 [a]		0.8	V
I_{XLKG}	X1 Leakage Current	$V_{IN} = V_{DD}$			400	µA
		$V_{IN} = V_{SS}$			–400	µA

a. Not tested. Guaranteed by design.

13.2.7 Group 7

Pin List:

$\overline{RI1}$, $\overline{RI2}$, $\overline{RING}$, SWITCH, $\overline{XDCS}$

$\overline{RING}$ and $\overline{XDCS}$ are back-drive protected.

TABLE 13-11. DC Characteristics of Group 7 Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input High Voltage [a]		2.0		V
V_{IL}	Input Low Voltage [a]			0.8	V
V_H	Hysteresis	$V_{BAT} = 3$ V	200		mV
I_{IL}	Input Leakage Current			100	µA

a. Not tested. Guaranteed by design.

13.2.8 Group 8

Pin List:

D7-0

TABLE 13-12. DC Characteristics of Group 8 Input Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input High Voltage		2.0	V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]	0.8	V
V_H	Hysteresis		250		mV

a. Not tested. Guaranteed by design.

TABLE 13-13. DC Characteristics of Group 8 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –15 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA		0.4	V

13.2.9 Group 9

Pin List:

$\overline{CS2,1}$, XD7,6, XD1,0

TABLE 13-14. DC Characteristics of Group 9 Input Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input High Voltage		2.0	V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]	0.8	V
V_H	Hysteresis		250		mV

a. Not tested. Guaranteed by design.

TABLE 13-15. DC Characteristics of Group 9 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –6 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA		0.4	V

13.2.10 Group 10

Pin List:

GPIO27-10, XD5-2

GPIO27-10 are back-drive protected.

TABLE 13-16. DC Characteristics of Group 10 Input Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input High Voltage		2.0	V_{DD}[a]	V
V_{IL}	Input Low Voltage		–0.5[a]	0.8	V
V_H	Hysteresis		250		mV

a. Not tested. Guaranteed by design.

TABLE 13-17. DC Characteristics of Group 10 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -2 mA [a]	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		0.4	V

a. I_{OH} is valid for a GPIO signal only when a it is not configured as open-drain.

13.2.11 Group 11

Pin List:

KBCLK, KBDAT, MCLK, MDAT

Output from these signals is open-drain and cannot be forced high.

TABLE 13-18. DC Characteristics of Group 11 Input Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input High Voltage		2.0	V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]	0.8	V
V_H	Hysteresis		250		mV

a. Not tested. Guaranteed by design.

TABLE 13-19. DC Characteristics of Group 11 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V

13.2.12 Group 12

Pin List:

P12, P16, P17, P20, P21.

TABLE 13-20. DC Characteristics of Group 12 Input Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input High Voltage		2.0	V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]	0.8	V
V_H	Hysteresis		250		mV

a. Not tested. Guaranteed by design.

TABLE 13-21. DC Characteristics of Group 12 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –2 mA [a]	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		0.4	V

a. I_{OH} is driven for 10 nsec after the low-to-high transition, on pins P12, P16 and P17.

13.2.13 Group 13

Pin List:

$\overline{AFD}$, $\overline{INIT}$, $\overline{SLIN}$, $\overline{STB}$.

TABLE 13-22. DC Characteristics of Group 13 Input Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input High Voltage		2.0	V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]	0.8	V
V_H	Hysteresis		250		mV

a. Not tested. Guaranteed by design.

TABLE 13-23. DC Characteristics of Group 13 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage [a]	I_{OH} = –2 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		0.4	V

a. Output from $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$, $\overline{SLIN}$ is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based (FIFO). (See Table 6-1 on page 85.) Otherwise, output from these signals is Level 2. External 4.7 KΩ pull-up resistors should be used.

13.2.14 Group 14

Pin List:

PD7-0

Group 14 pins are back-drive protected.

TABLE 13-24. DC Characteristics of Group 14 Input Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input High Voltage		2.0	V_{DD} [a]	V
V_{IL}	Input Low Voltage		–0.5 [a]	0.8	V
V_H	Hysteresis		250		mV

a. Not tested. Guaranteed by design.

TABLE 13-25. DC Characteristics of Group 14 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage [a]	I_{OH} = –2 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		0.4	V

a. Output from PD7-0 is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based (FIFO) and bit 4 of the Control2 parallel port register is 1. (See Table 6-1 on page 85.) Otherwise, output from these signals is Level 2. External 4.7 KΩ pull-up resistors should be used.

13.2.15 Group 15

Pin List:

IRQ1,3,4,5,6,7,8,9,10,11,12,14,15

TABLE 13-26. DC Characteristics of Group 15 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –15 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA		0.4	V
V_H	Hysteresis		250		mV

13.2.16 Group 16

Pin List:

DENSEL, $\overline{\text{DIR}}$, $\overline{\text{DR1,0}}$, $\overline{\text{HDSEL}}$, $\overline{\text{MTR1,0}}$, $\overline{\text{STEP}}$, $\overline{\text{WDATA}}$, $\overline{\text{WGATE}}$

TABLE 13-27. DC Characteristics of Group 16 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –4 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 40 mA		0.4	V

13.2.17 Group 17

Pin List:

BOUT2,1, $\overline{DTR2,1}$, IRSL2-0, $\overline{RTS2,1}$, SOUT2,1.

TABLE 13-28. DC Characteristics of Group 17 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –6 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA		0.4	V
V_H	Hysteresis			250	mV

13.2.18 Group 18

Pin List:

DRQ3-0

TABLE 13-29. DC Characteristics of Group 18 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –15 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA		0.4	V

13.2.19 Group 19

Pin List:

IRTX

TABLE 13-30. DC Characteristics of Group 19 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –6mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA		0.4	V

13.2.20 Group 20

Pin List:

DRATE0

TABLE 13-31. DC Characteristics of Group 20 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –6 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 6 mA		0.4	V

13.2.21 Group 21

Pin List:

$\overline{CS0}$, $\overline{CSOUT}$, $\overline{POR}$

TABLE 13-32. DC Characteristics of Group 21 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	Open-Drain			
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		0.4	V

13.2.22 Group 22

Pin List:

$\overline{IOCHRDY}$, $\overline{ZWS}$

TABLE 13-33. DC Characteristics of Group 22 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –15 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA		0.4	V

13.2.23 Group 23

Pin List:

$\overline{ONCTL}$

This pin is back-drive protected and open-drain. V_{OH} is not tested for $\overline{ONCTL}$.

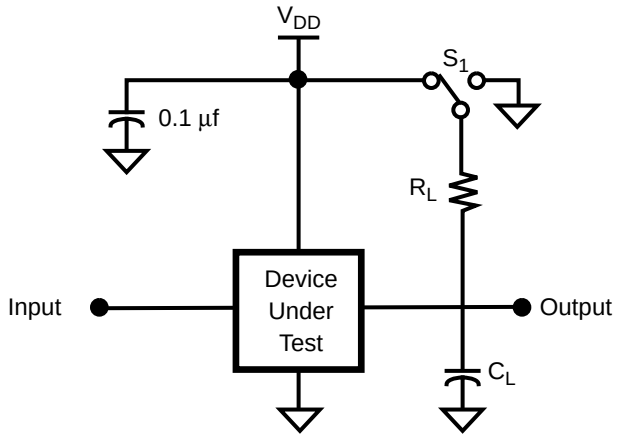
TABLE 13-34. DC Characteristics of Group 23 Output Pins

Symbol	Parameter	Conditions	Min	Max	Units
V_{OL}	Output Low Voltage	I_{OL} = 14 mA		0.4	V

13.3 AC ELECTRICAL CHARACTERISTICS

13.3.1 AC Test Conditions T_A = 0 °C to 70 °C, V_{DD} = 5.0 V ±10%

Load Circuit (Notes 1, 2, 3)



AC Testing Input, Output Waveform

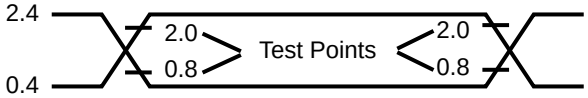


FIGURE 13-1. AC Test Conditions, T_A = 0 °C to 70 °C, V_{DD} = 5.0 V ±10%

Notes:

1. C_L = 100 pF, includes jig and scope capacitance.
2. S_1 = Open for push-pull output pins.
   S_1 = V_{DD} for high impedance to active low and active low to high impedance measurements.
   S_1 = GND for high impedance to active high and active high to high impedance measurements.
   R_L = 1.0 KΩ for µP interface pins.
3. For the FDC open drive interface pins, S_1 = V_{DD} and R_L = 150Ω.

13.3.2 Clock Timing

TABLE 13-35. Clock Timing

Symbol	Parameter	24MHz		48MHz		Unit
		Min	Max	Min	Max	
t_{CH}	Clock High Pulse Width [a]	16		8.4		nsec
t_{CL}	Clock Low Pulse Width [a]	16		8.4		nsec
f_{TOL}	Clock Frequency Tolerance	±100		±200		ppm
t_{ICP}	Internal Clock Period (See Table 13-36.)					
t_{DRP}	Data Rate Period (See Table 13-36.)					

a. Not tested. Guaranteed by design.

TABLE 13-36. Nominal t_{ICP}, t_{DRP} Values

MFM Data Rate	t_{DRP}	t_{ICP}	Value	Unit
1 Mbps	1000	3 x t_{CP}	125	nsec
500 Kbps	2000	3 x t_{CP}	125	nsec
300 Kbps	3333	5 x t_{CP}	208	nsec
250 Kbps	4000	6 x t_{CP}	250	nsec

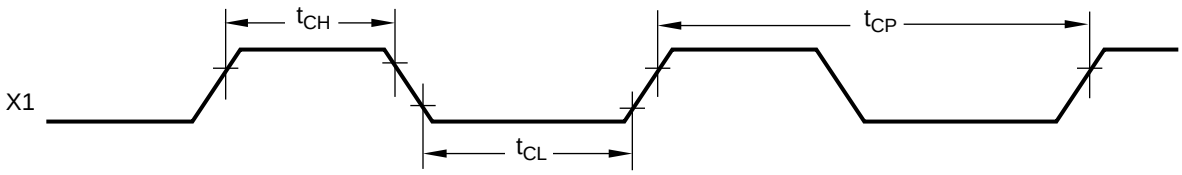


FIGURE 13-2. Clock Timing

13.3.3 Microprocessor Interface Timing

TABLE 13-37. Microprocessor Interface Timing

Symbol	Parameter	Min	Max	Unit
t_{AR}	Valid Address to Read Active	18		nsec
t_{AW}	Valid Address to Write Active	18		nsec
t_{DH}	Data Hold	0		nsec
t_{DS}	Data Setup	18		nsec
t_{HZ}	Read to Floating Data Bus [a]	13	25	nsec
t_{PS}	Port Setup	10		nsec
t_{RA}	Address Hold from Inactive Read	0		nsec
t_{RCU}	Read Cycle Update [a]	45		nsec
t_{RD}	Read Strobe Width	60		nsec
t_{RDH}	Read Data Hold	10		nsec
t_{RI}	Read Strobe to Clear IRQ6		55	nsec
t_{RVD}	Active Read to Valid Data		55	nsec
t_{WA}	Address Hold from Inactive Write	0		nsec
t_{WCU}	Write Cycle Update [a]	45		nsec
t_{WI}	Write Strobe to Clear IRQ6		55	nsec
t_{WO}	Write Data to Port Update		60	nsec
t_{WR}	Write Strobe Width	60		nsec
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RCU}$ [a]	123		nsec
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$ [a]	123		nsec
t_{WRR}	$\overline{RD}$ low after $\overline{WR}$ high [a]	80		nsec

a. Not tested. Guaranteed by design.

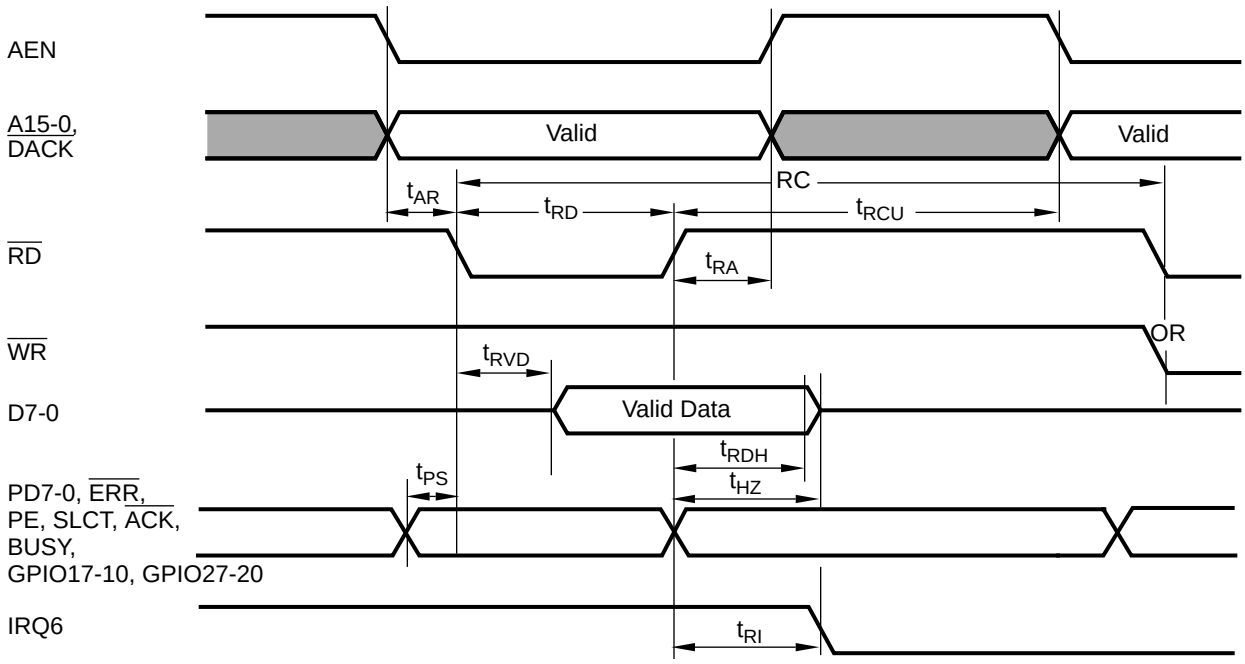


FIGURE 13-3. Microprocessor Read Timing

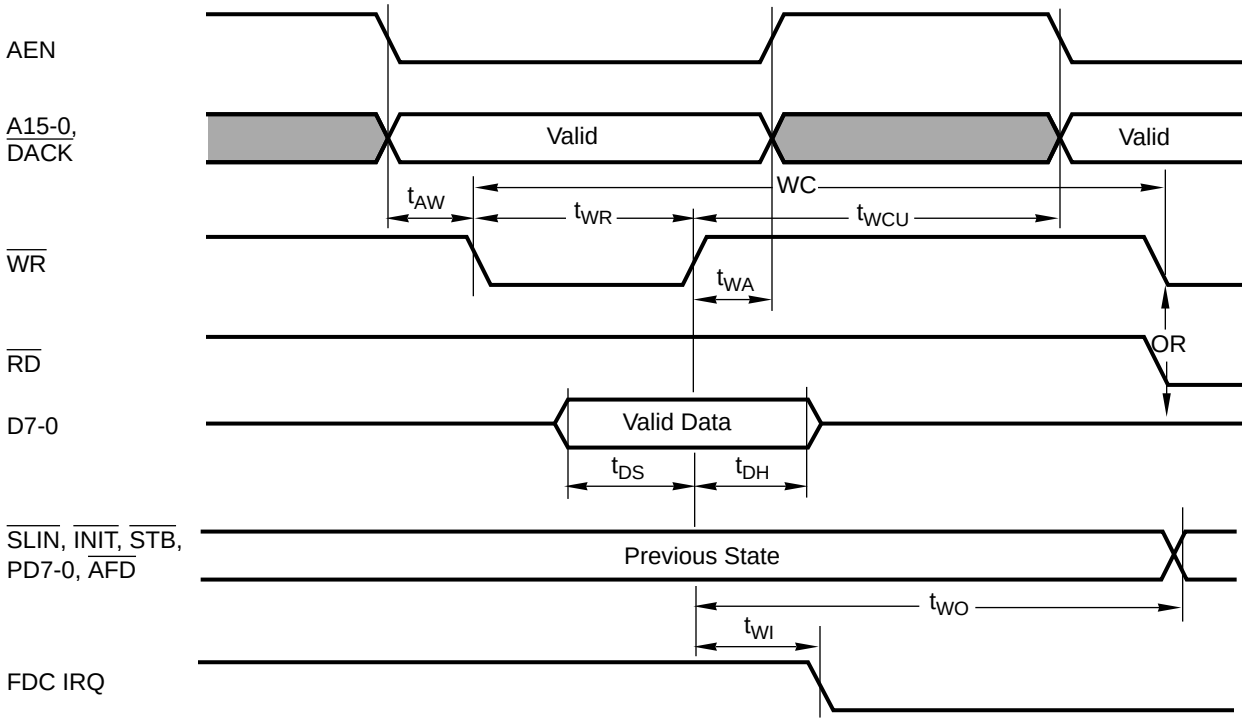


FIGURE 13-4. Microprocessor Write Timing

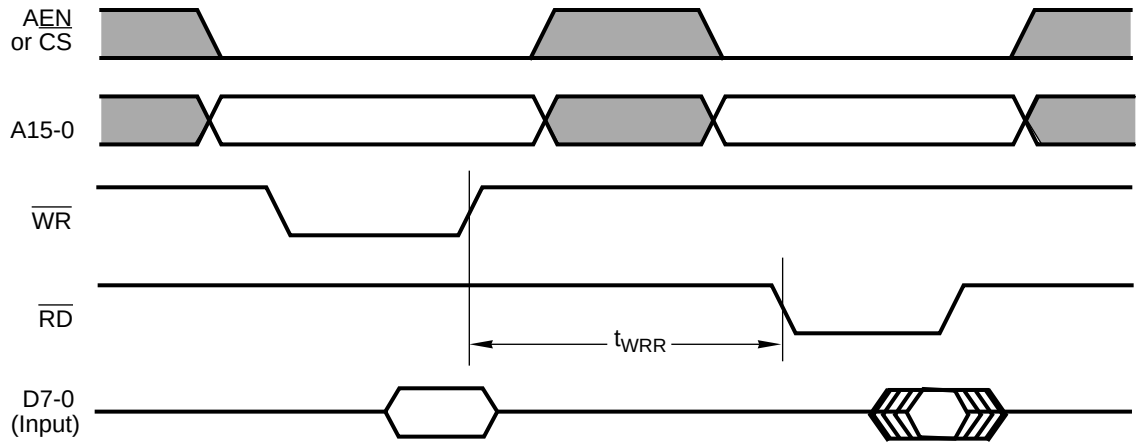


FIGURE 13-5. Read After Write Operation to All Registers and RAM

13.3.4 Baud Output Timing

TABLE 13-38. Baud Output Timing

Symbol	Parameter	Conditions	Min	Max	Unit
N	Baud Divisor		1	65535	nsec
t_{BHD}	Baud Output Positive Edge Delay [a]	CLK = 24 MHz/2, 100 pF load		56	nsec
t_{BLD}	Baud Output Negative Edge Delay [a]	CLK = 24 MHz/2, 100 pF load		56	nsec

a. Not tested. Guaranteed by design.

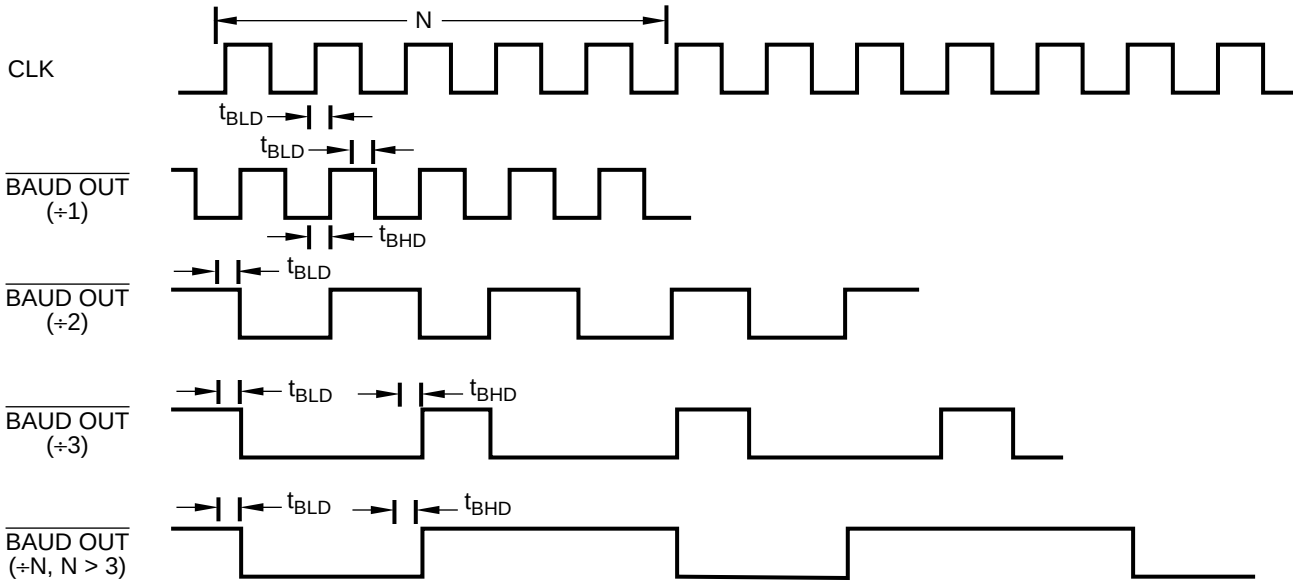


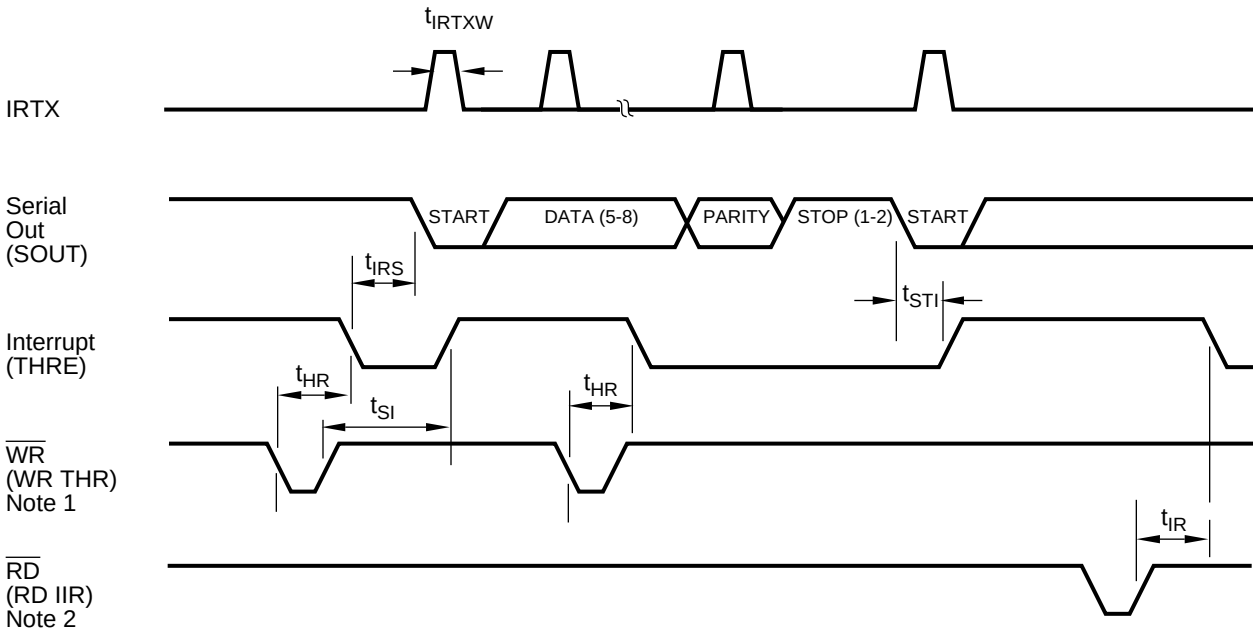
FIGURE 13-6. Baud Output Timing

13.3.5 Transmitter Timing

TABLE 13-39. Transmitter Timing

Symbol	Parameter	Min	Max	Unit
t_{IRTXW}	IRTX Pulse Width	1.6 µsec	$^3/_{16}$	Baud Output Cycles
t_{HR}	Delay from $\overline{WR}$ (WR THR) to Reset IRQ		40	nsec
t_{IR}	Delay from $\overline{RD}$ (RD IIR) to Reset IRQ (THRE)		55	nsec
t_{IRS}	Delay from initial IRQ Reset to Transmit Start [a]	8	24	Baud Output Cycles
t_{SI}	Delay from Initial Write to IRQ [a]	16	24	Baud Output Cycles
t_{STI}	Delay from Start Bit to IRQ (THRE) [a]		8	Baud Output Cycles

a. Not tested. Guaranteed by design.



Notes:

1. See write cycle timing in Figure 13-4.
2. See read cycle timing in Figure 13-3.

FIGURE 13-7. Transmitter Timing

13.3.6 Receiver Timing

TABLE 13-40. Receiver Timing

Symbol	Parameter	Conditions	Min	Max	Unit
t_{IRRXW}	IRRX Pulse Width [a]		1.6 µsec	$^{6}/_{16}$	Baud Output Cycles
t_{RAI1}	Delay from Active Edge of $\overline{RD}$ to Reset IRQ			78	nsec
t_{RAI2}	Delay from Active Edge of $\overline{RD}$ to Reset IRQ			78	nsec
t_{RAI3}	Delay from Active Edge of $\overline{RD}$ to Reset IRQ			78	nsec
t_{RINT}	Delay from Inactive Edge of $\overline{RD}$ (RD LSR) to reset IRQ			55	nsec
t_{SCD}	Delay from RCLK to sample time	b		41	nsec
t_{SINT}	Delay from Stop bit to Set Interrupt [a]			2	Baud Output Cycles

a. Not tested. Guaranteed by design.
b. This is internal timing and is therefore not tested.

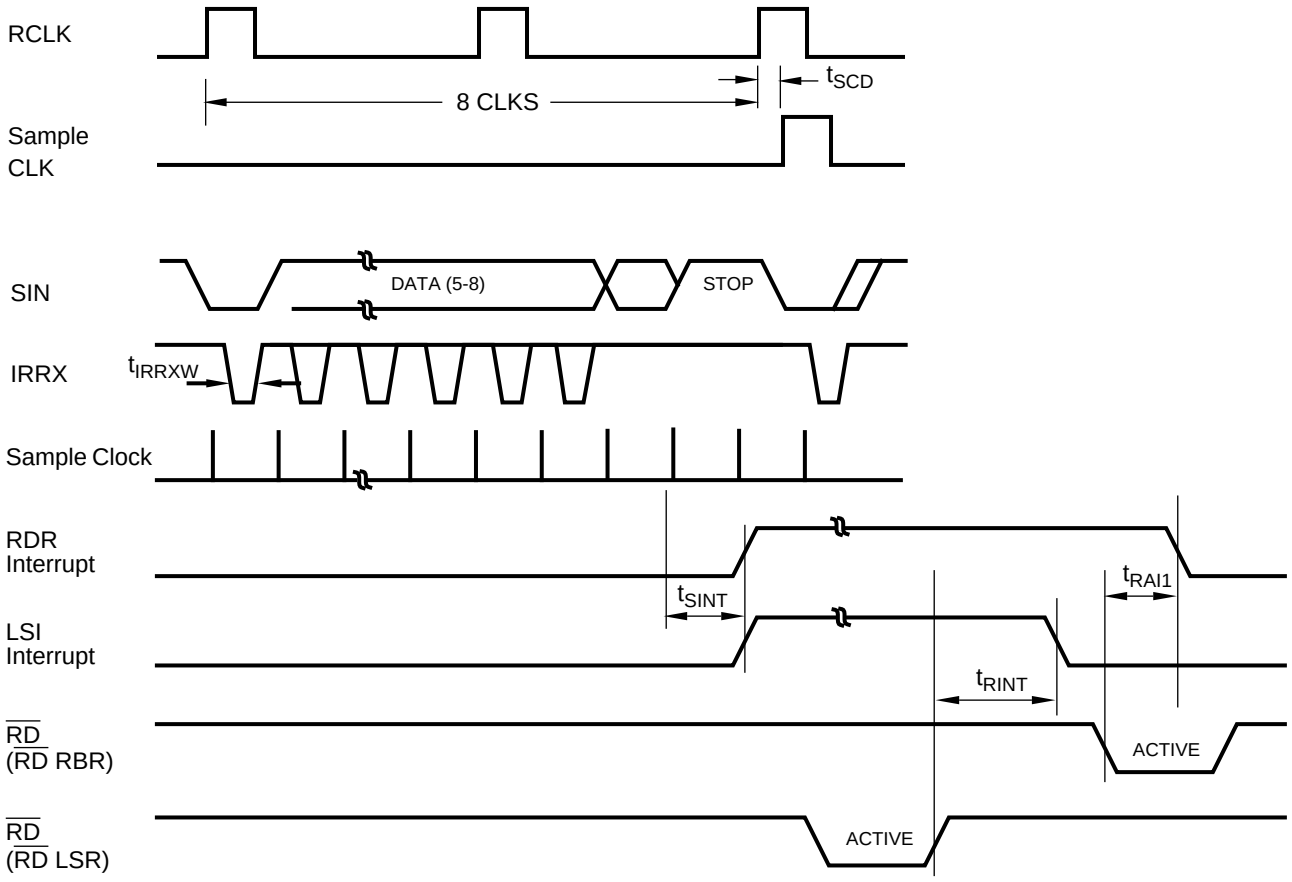
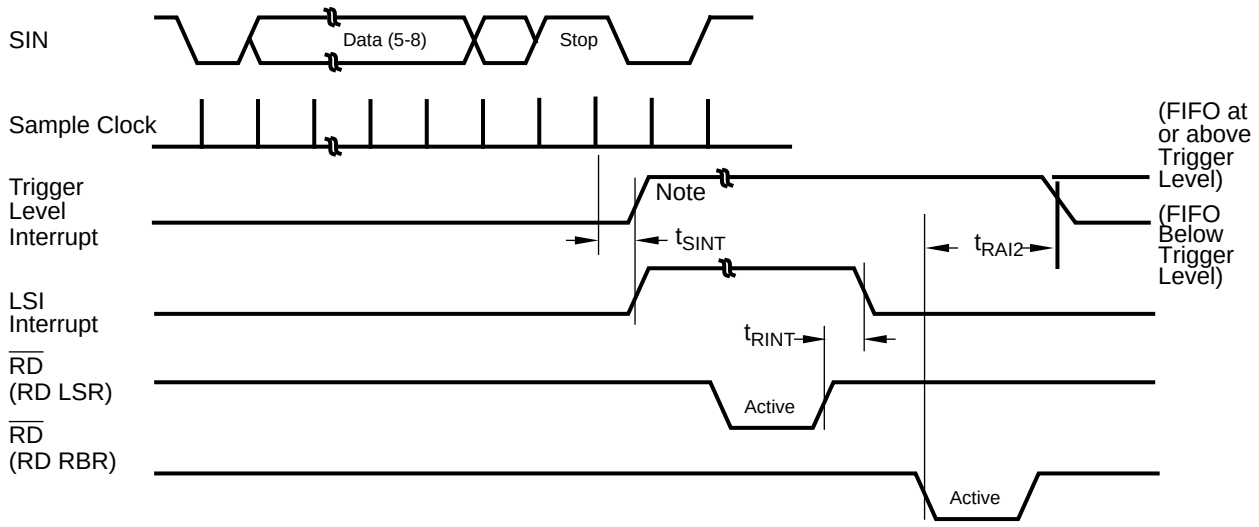


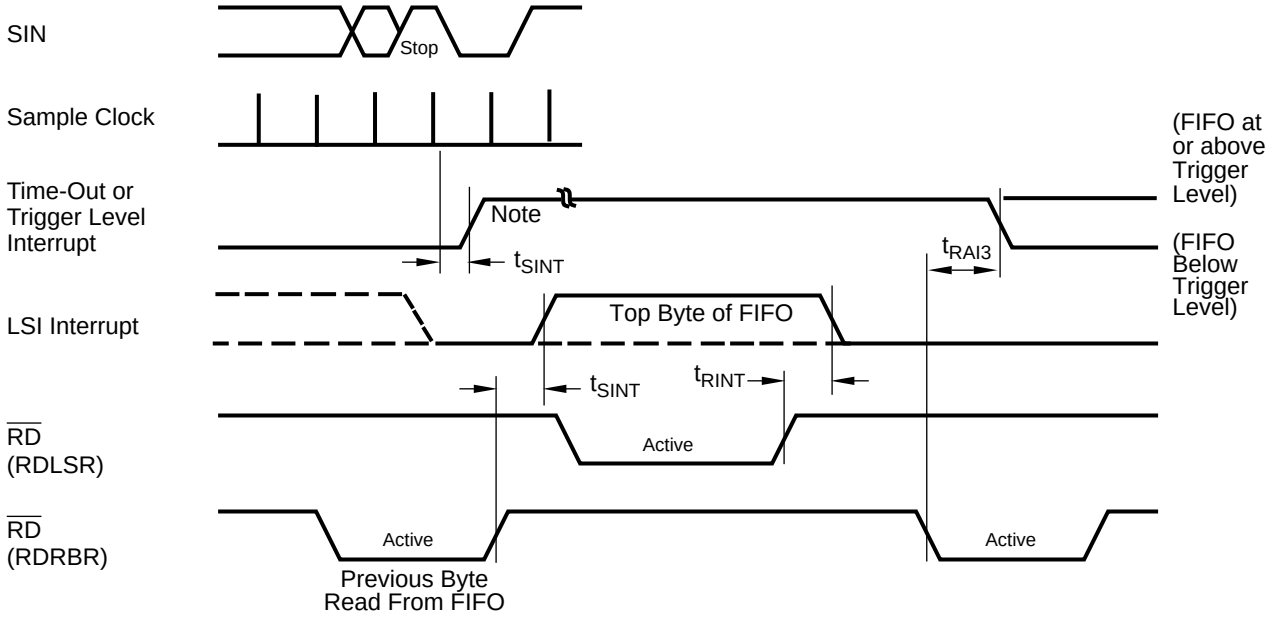
FIGURE 13-8. Receiver Timing



Note:

If SCR0 = 1, then t_{SINT} = 3 RCLKs. For a time-out interrupt, t_{SINT} = 8 RCLKs.

FIGURE 13-9. FIFO Mode Receiver Timing



Note:

If SCR0 = 1, then t_{SINT} = 3 RCLKs. For a time-out interrupt, t_{SINT} = 8 RCLKs

FIGURE 13-10. Time-Out Receiver Timing

13.3.7 UART, Sharp-IR and Consumer-IR Timing

TABLE 13-41. UART, Sharp-IR and Consumer-IR Timing

Symbol	Parameter	Conditions	Min	Max	Unit
t_{BT}	Single Bit Time in UART and Sharp-IR	Transmitter	$t_{BTN} - 30$ [a]	$t_{BTN} + 30$	nsec
		Receiver	$t_{BTN} - 2\%$	$t_{BTN} + 2\%$	nsec
t_{CMW}	Modulation Signal Pulse Width in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CWN} - 30$ [b]	$t_{CWN} + 30$	nsec
		Receiver	500		nsec
t_{CMP}	Modulation Signal Period in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CPN} - 30$ [c]	$t_{CPN} + 30$	nsec
		Receiver	t_{MMIN} [d]	t_{MMAX} [d]	nsec

a. t_{BTN} is the nominal bit time in UART, Sharp-IR, SIR and Consumer Remote Control modes. It is determined by the setting of the Baud Rate Generator Divisor registers P_BGDL and P_BGDH at offsets 00h and 01h, respectively, in bank 5 of logical device 5.

b. t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCPW field (bits 7-5) of the IRTXMC register at offset 01h and the TXHSC bit (bit 2) in the RCCFG register at offset 02h. Both registers are in bank 7 of logical device 5.

c. t_{CPN} is the nominal period of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCFREQ field (bits 4-0) of the IRTXMC register at offset 01h and the TXHSC bit (bit 2) of the RCCFG register at offset 02h. Both registers are in bank 7 of logical device 5.

d. t_{MMIN} and t_{MMAX} define the time range within which the period of the incoming carrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the content of register IRRXDC at offset 00h and the setting of the RXHSC bit (bit 5) in the RCCFG register at offset 02h. Both registers are in bank 7 of logical device 5.

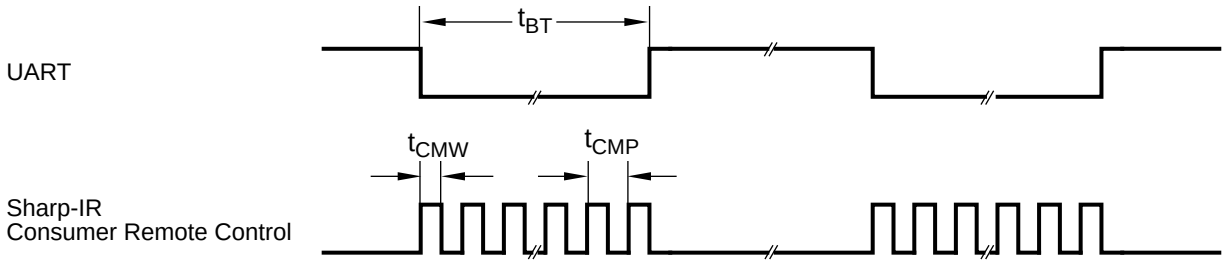


FIGURE 13-11. UART, Sharp-IR and Consumer Remote Control Timing

13.3.8 SIR, MIR and FIR Timing

TABLE 13-42. SIR, MIR and FIR Timing

Symbol	Parameter	Conditions	Min	Max	Unit
t_{SPW}	SIR Signal Pulse Width	Transmitter, Variable	$(^3/_{16})$ x t_{BTN} – 25 [a]	$(^3/_{16})$ x t_{BTN} – 25	nsec
		Transmitter, Fixed	1.60	1.65	µsec
		Receiver	1		µsec
S_{DRT}	SIR Transmitter Data Rate Tolerance			± 0.87 %	
t_{SJT}	SIR Receiver Edge Jitter, % of Nominal Bit Duration			± 6.5 %	
t_{MPW}	MIR Signal Pulse Width	Transmitter	t_{MWN} – 25 [b]	t_{MWN} + 25	nsec
		Receiver	60		nsec
M_{DRT}	MIR Transmitter Data Rate Tolerance			± 0.1 %	
t_{MJT}	MIR Receiver Edge Jitter, % of Nominal Bit Duration			± 2.9 %	
t_{FPW}	FIR Signal Pulse Width	Transmitter	120	130	nsec
		Receiver	90	160	nsec
t_{FDPW}	FIR Signal Double Pulse Width	Transmitter	245	255	nsec
		Receiver	215	285	nsec
F_{DRT}	FIR Transmitter Data Rate Tolerance			± 0.01 %	
t_{FJT}	FIR Receiver Edge Jitter, % of Nominal Bit Duration			± 4.0 %	

a. t_{BTN} is the nominal bit time in UART, Sharp-IR, SIR and Consumer Remote Control modes. It is determined by the settings of the Baud Rate Generator Divisor registers P_BGDL and P_BGDH at offsets 00h and 01h, respectively, in bank 5 of logical device 5.

b. t_{MWN} is the nominal pulse width for MIR mode. It is determined by the M_PWID field (bits 4-0) in the MIR_PW register at offset 01h in bank 6 of logical device 5.

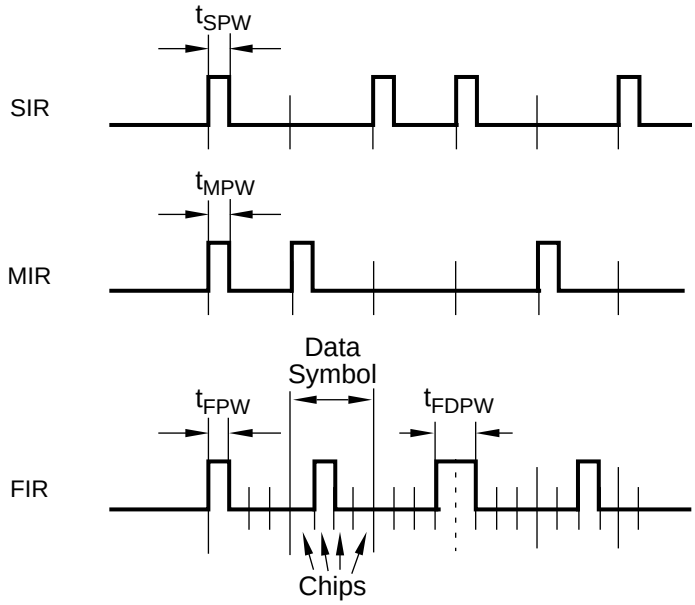


FIGURE 13-12. SIR, MIR and FIR Timing

13.3.9 IRSLn Write Timing

TABLE 13-43. IRSLn Write Timing

Symbol	Parameter	Conditions	Min	Max	Unit
t_{WOD}	IRSLn Output Delay from Write Inactive			60	nsec

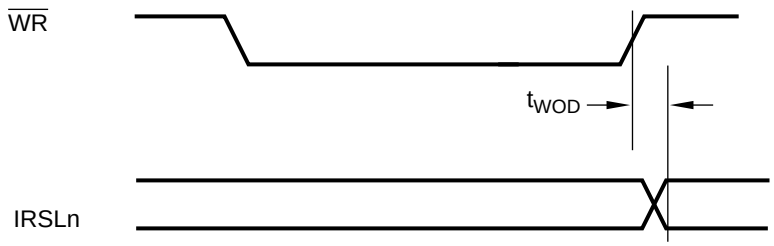
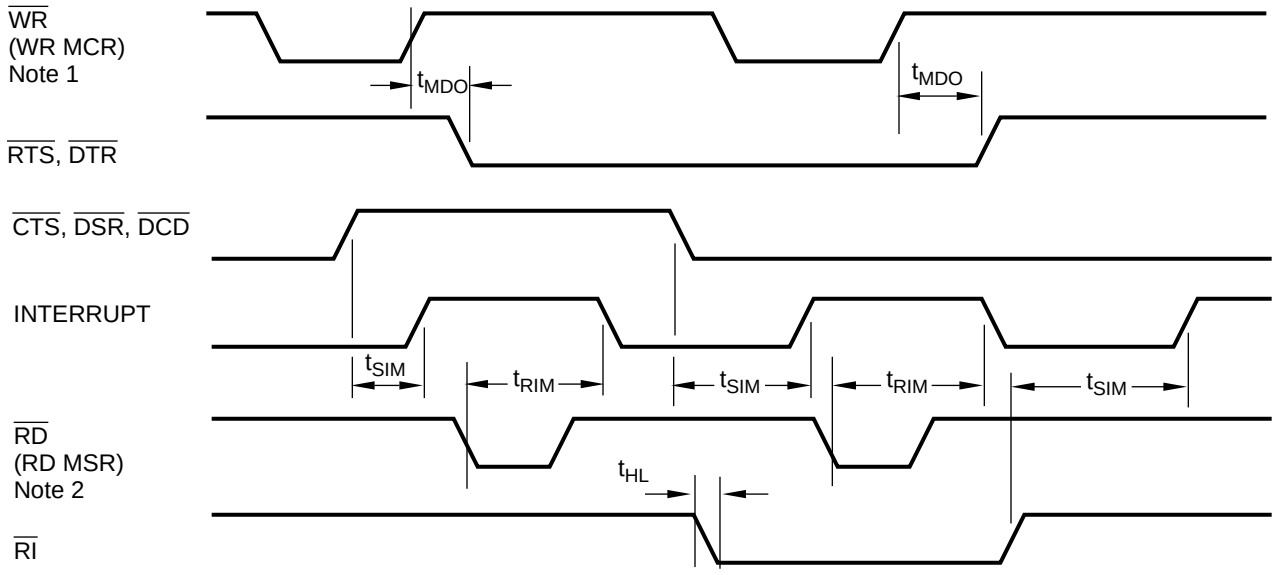


FIGURE 13-13. IRSLn Write Timing

13.3.10 Modem Control Timing

TABLE 13-44. Modem Control Timing

Symbol	Parameter	Conditions	Min	Max	Unit
t_{HL}	$\overline{RI2,1}$ High to Low Transition		10		nsec
t_{MDO}	Delay from $\overline{WR}$ (WR MCR) to Output			40	nsec
t_{RIM}	Delay to Reset IRQ from $\overline{RD}$ (RD MSR)			78	nsec
t_{SIM}	Delay to Set IRQ from Modem Input			40	nsec



Notes:

1. See write cycle timing, Figure 13-4.
2. See read cycle timing, Figure 13-3.

FIGURE 13-14. Modem Control Timing

13.3.11 DMA Timing

TABLE 13-45. FDC DMA Timing

Symbol	Parameter	Min	Max	Unit
t_{KI}	$\overline{DACK}$ Inactive Pulse Width	25		nsec
t_{KK}	$\overline{DACK}$ Active Pulse Width	65		nsec
t_{KQ}	$\overline{DACK}$ Active Edge to DRQ Inactive		65	nsec
t_{QK}	DRQ to $\overline{DACK}$ Active Edge	10		nsec
t_{QP}	DRQ Period (Except Non-Burst DMA) [a]	8 x t_{DRP}		
t_{QQ}	DRQ Inactive Non-Burst Pulse Width	300	400 [b]	nsec
t_{QR}	DRQ to $\overline{RD}$, $\overline{WR}$ Active	15		nsec
t_{QW}	DRQ to End of $\overline{RD}$, $\overline{WR}$ [a c] (DRQ Service Time)		(8 x t_{DRP}) – (16 x t_{ICP})	
t_{QT}	DRQ to TC Active [a c] (DRQ Service Time)		(8 x t_{DRP}) – (16 x t_{ICP})	
t_{RQ}	$\overline{RD}$, $\overline{WR}$ Active Edge to DRQ Inactive [d]		65	nsec
t_{TQ}	TC Active Edge to DRQ Inactive		75	nsec
t_{TT}	TC Active Pulse Width	50		nsec

a. t_{DRP} and t_{ICP} are defined in Table 13-36.
b. Only in case of pending DRQ.
c. Values shown are with the FIFO disabled, or with FIFO enabled and THRESH = 0. For nonzero values of THRESH, add (THRESH x 8 x t_{DRP}) to the values shown.
d. The active edge of $\overline{RD}$ or $\overline{WR}$ and TC is recognized only when $\overline{DACK}$ is active.

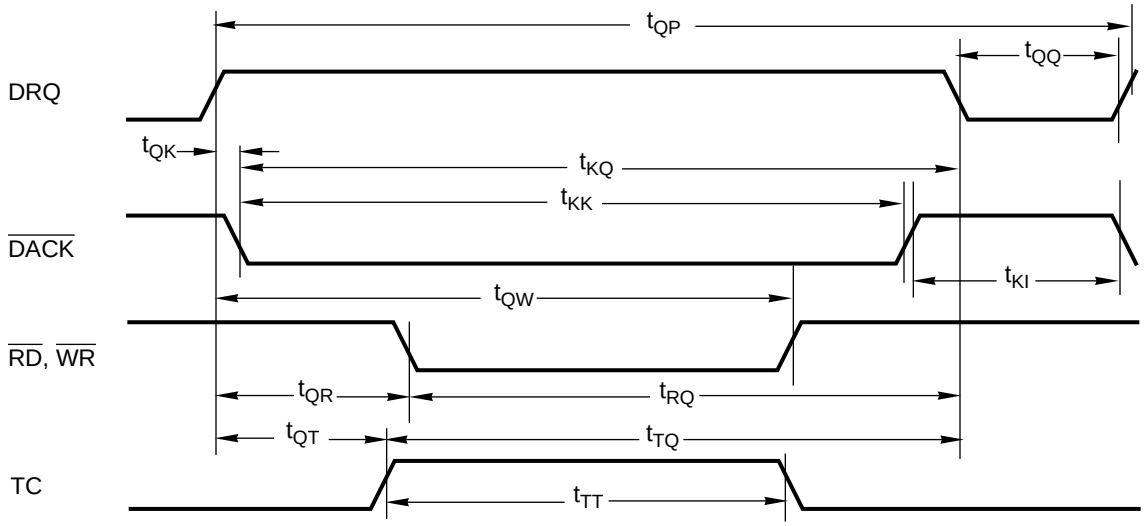


FIGURE 13-15. FDC DMA Timing

TABLE 13-46. ECP DMA Timing

Symbol	Parameter	Min	Max	Unit
t_{KIP}	$\overline{DACK}$ Inactive Pulse Width	25		nsec
t_{KKP}	$\overline{DACK}$ Active Pulse Width	65		nsec
t_{KQP}	$\overline{DACK}$ Active Edge to DRQ Inactive [a b]		65 + (6 x 32 x t_{CP})	nsec
t_{QKP}	DRQ to $\overline{DACK}$ Active Edge	10		nsec
t_{QPP}	DRQ Period	330		nsec
t_{QQP}	DRQ Inactive Non-Burst Pulse Width	300	400 [c]	nsec
t_{QRP}	DRQ to $\overline{RD}$, $\overline{WR}$ Active	15		nsec
t_{RQP}	$\overline{RD}$, $\overline{WR}$ Active Edge to DRQ Inactive [d]		65	nsec
t_{TQP}	TC Active Edge to DRQ Inactive		75	nsec
t_{TT}	TC Active Pulse Width	50		nsec

a. One DMA transaction takes six clock cycles.
b. t_{CP} is defined in Table 13-35.
c. Only in case of pending DRQ.
d. The active edge of $\overline{RD}$ or $\overline{WR}$ and TC is recognized only when $\overline{DACK}$ is active.

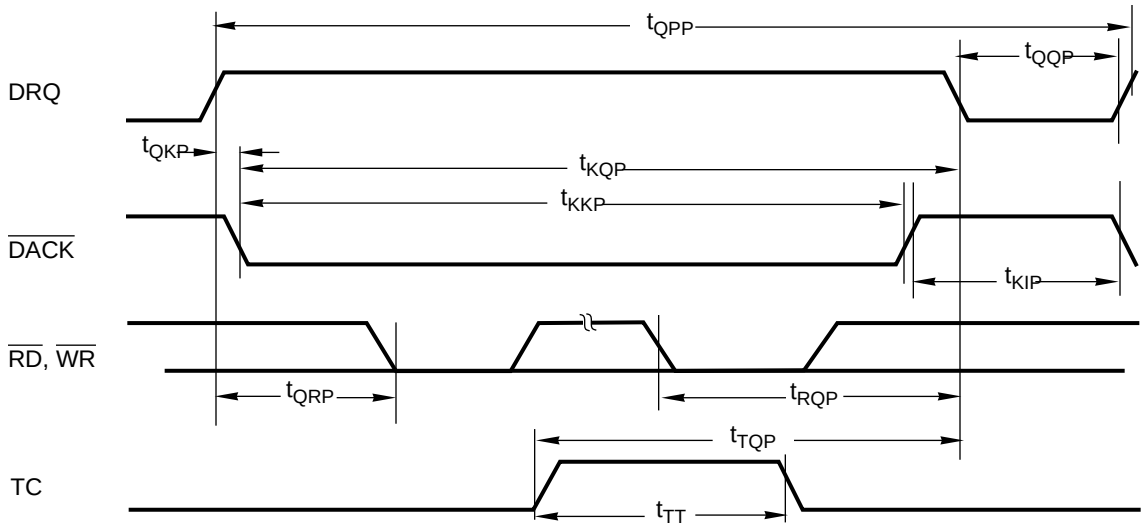


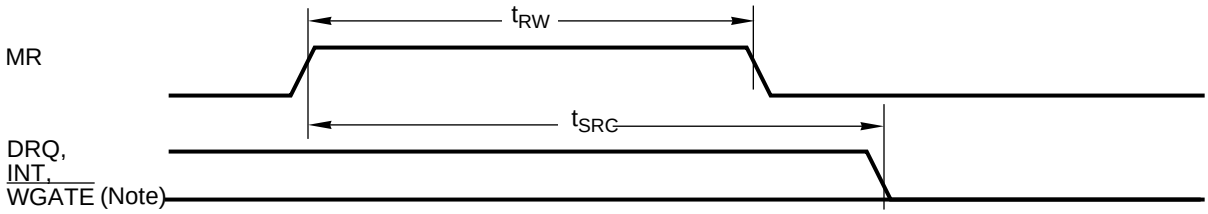
FIGURE 13-16. ECP DMA Timing

13.3.12 Reset Timing

TABLE 13-47. Reset Timing

Symbol	Parameter	Min	Max	Unit
t_{RW}	Reset Width [a]	100		µsec
t_{SRC}	Reset to Control Inactive [b]		300	nsec

a. The software reset pulse width is 100 nsec.
b. Not tested. Guaranteed by design.



Note:
In PC-AT mode, the DRQ and IRQ signals of the FDC are in TRI-STATE after time t_{SRC}.

FIGURE 13-17. Reset Timing

13.3.13 Write Data Timing

TABLE 13-48. Write Data Timing

Symbol	Parameter	Min	Max	Unit
t_{HDH}	$\overline{HDSEL}$ Hold from $\overline{WGATE}$ Inactive[a]	750		µsec
t_{HDS}	$\overline{HDSEL}$ Setup to $\overline{WGATE}$ Active[a]	100		µsec
t_{WDW}	Write Data Pulse Width	Table 13-49		

a. Not tested. Guaranteed by design.

TABLE 13-49. Write Data Timing – Minimum t_{WDW} Values

Data Rate	t_{DRP}	t_{WDW}	t_{WDW} Value	Unit
1 Mbps	1000	2 x t_{ICP} [a]	250	nsec
500 Kbps	2000	2 x t_{ICP} [a]	250	nsec
300 Kbps	3333	2 x t_{ICP} [a]	375	nsec
250 Kbps	4000	2 x t_{ICP} [a]	500	nsec

a. t_{ICP} is the internal clock period defined in Table 13-36.

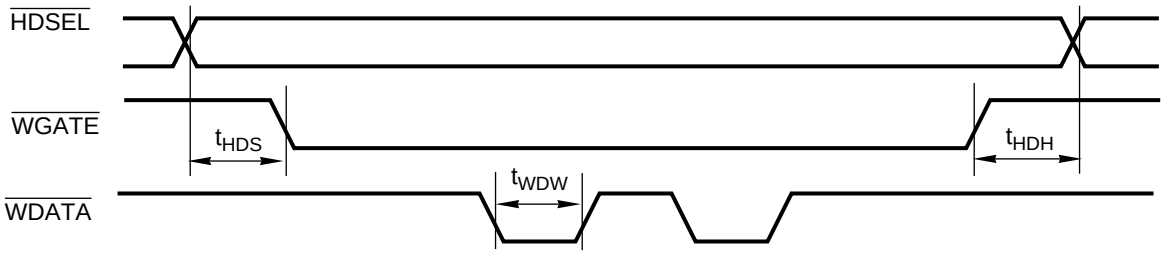


FIGURE 13-18. Write Data Timing

13.3.14 Drive Control Timing

TABLE 13-50. Drive Control Timing

Symbol	Parameter	Min	Max	Unit
t_{DRV}	$\overline{DR1,0}$ and $\overline{MTR1,0}$ from End of $\overline{WR}$		110	nsec
t_{DST}	$\overline{DIR}$ Setup to $\overline{STEP}$ Active	6		µsec
t_{IW}	Index Pulse Width	100		nsec
t_{STD}	$\overline{DIR}$ Hold from $\overline{STEP}$ Inactive	t_{STR}		msec
t_{STP}	$\overline{STEP}$ Active High Pulse Width	8		µsec
t_{STR}	$\overline{STEP}$ Rate Time (See Table 5-24 on page 93.)	1		msec

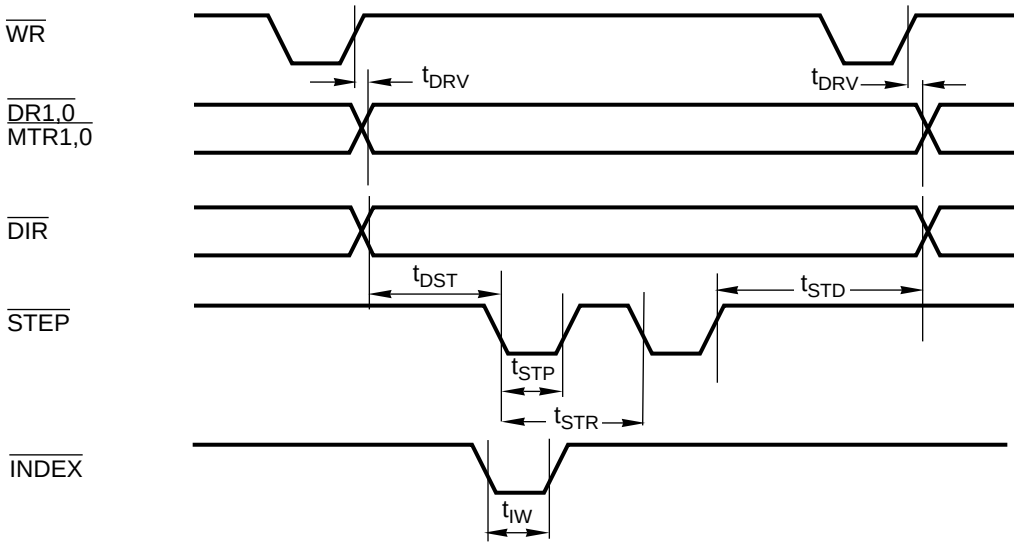


FIGURE 13-19. Drive Control Timing

13.3.15 Read Data Timing

TABLE 13-51. Read Data Timing

Symbol	Parameter	Min	Max	Unit
t_{RDW}	Read Data Pulse Width	50		nsec

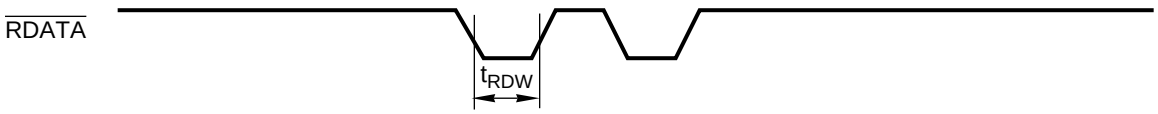


FIGURE 13-20. Read Data Timing

13.3.16 Parallel Port Timing

TABLE 13-52. Standard Parallel Port Timing

Symbol	Parameter	Conditions	Typical	Max	Unit
t_{PDH}	Port Data Hold	These times are system dependent and are therefore not tested.	500		nsec
t_{PDS}	Port Data Setup	These times are system dependent and are therefore not tested.	500		nsec
t_{PILa}	Port Active Low Interrupt, Active			33	nsec
t_{PILia}	Port Active Low Interrupt, Inactive			33	nsec
t_{PIHa}	Port Active High Interrupt, Active			33	nsec
t_{PIHia}	Port Active High Interrupt, Inactive			33	nsec
t_{PIz}	Port Active High Interrupt, TRI-STATE			33	nsec
t_{SW}	Strobe Width	These times are system dependent and are therefore not tested.	500		nsec

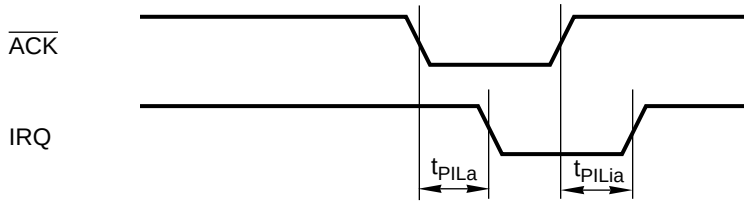


FIGURE 13-21. Parallel Port Interrupt Timing (Compatible Mode)

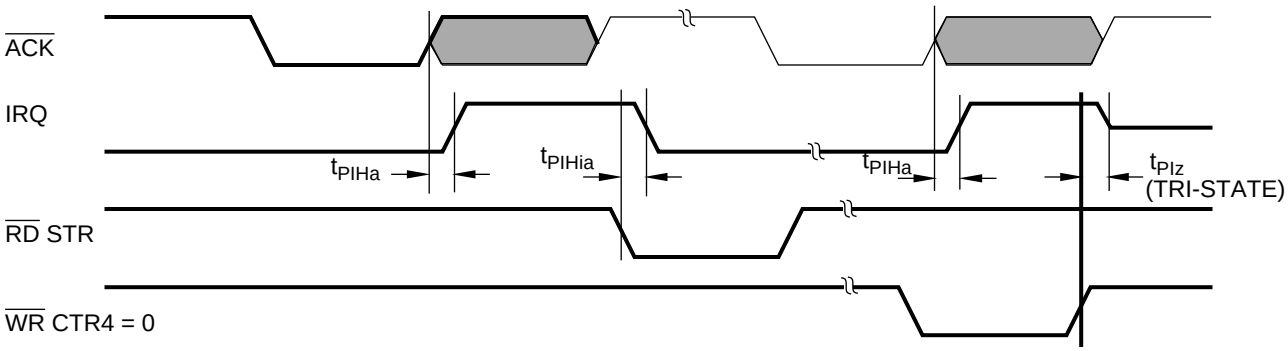


FIGURE 13-22. Parallel Port Interrupt Timing (Extended Mode)

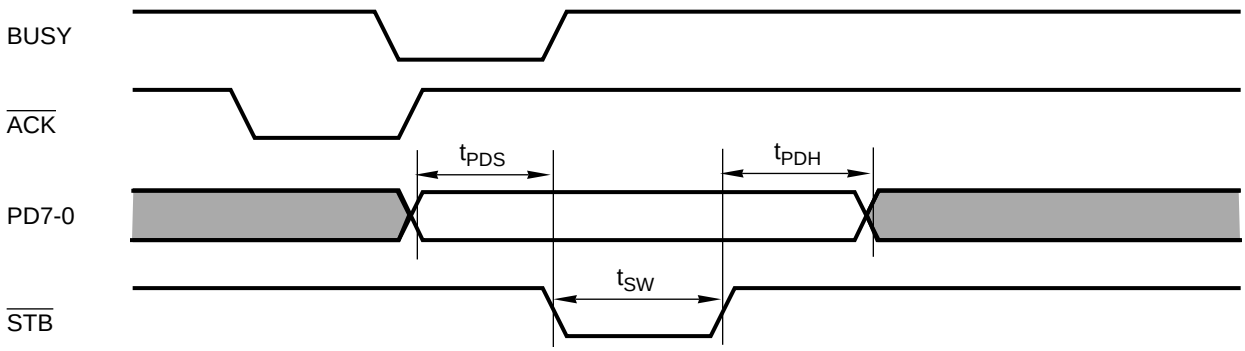


FIGURE 13-23. Typical Parallel Port Data Exchange

13.3.17 Enhanced Parallel Port 1.7 Timing

TABLE 13-53. Enhanced Parallel Port 1.7 Timing Parameters

Symbol	Parameter	Notes	Min	Max	Unit
t_{WW17}	$\overline{WRITE}$ Active or Inactive from $\overline{WR}$ Active or Inactive			45	nsec
t_{WST17}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active or Inactive from $\overline{WR}$ or $\overline{RD}$ Active or Inactive	a		45	nsec
t_{WEST17}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active after $\overline{WRITE}$ Becomes Active		0		nsec
t_{WPD17h}	PD7-0 Hold after $\overline{WRITE}$ Becomes Inactive		50		nsec
t_{HRW17}	IOCHRDY Active or Inactive after $\overline{WAIT}$ Becomes Active or Inactive			40	nsec
t_{WPDS17}	PD7-0 Valid after $\overline{WRITE}$ Becomes Active	b		15	nsec
t_{EPDW17}	PD7-0 Valid Width		80		nsec
t_{EPD17h}	PD7-0 Hold after $\overline{DSTRB}$ or $\overline{ASTRB}$ Becomes Inactive		0		nsec
t_{ZWS17a}	$\overline{ZWS}$ Valid after $\overline{WR}$ or $\overline{RD}$ Active			45	nsec
t_{ZWS17h}	$\overline{ZWS}$ Hold after $\overline{WR}$ or $\overline{RD}$ Inactive		0		nsec

a. The PC87308VUL design guarantees that $\overline{WRITE}$ will not change from low to high before $\overline{DSTRB}$, or $\overline{ASTRB}$, goes from low to high.
b. D7-0 is stable 15 nsec before $\overline{WR}$ becomes active.

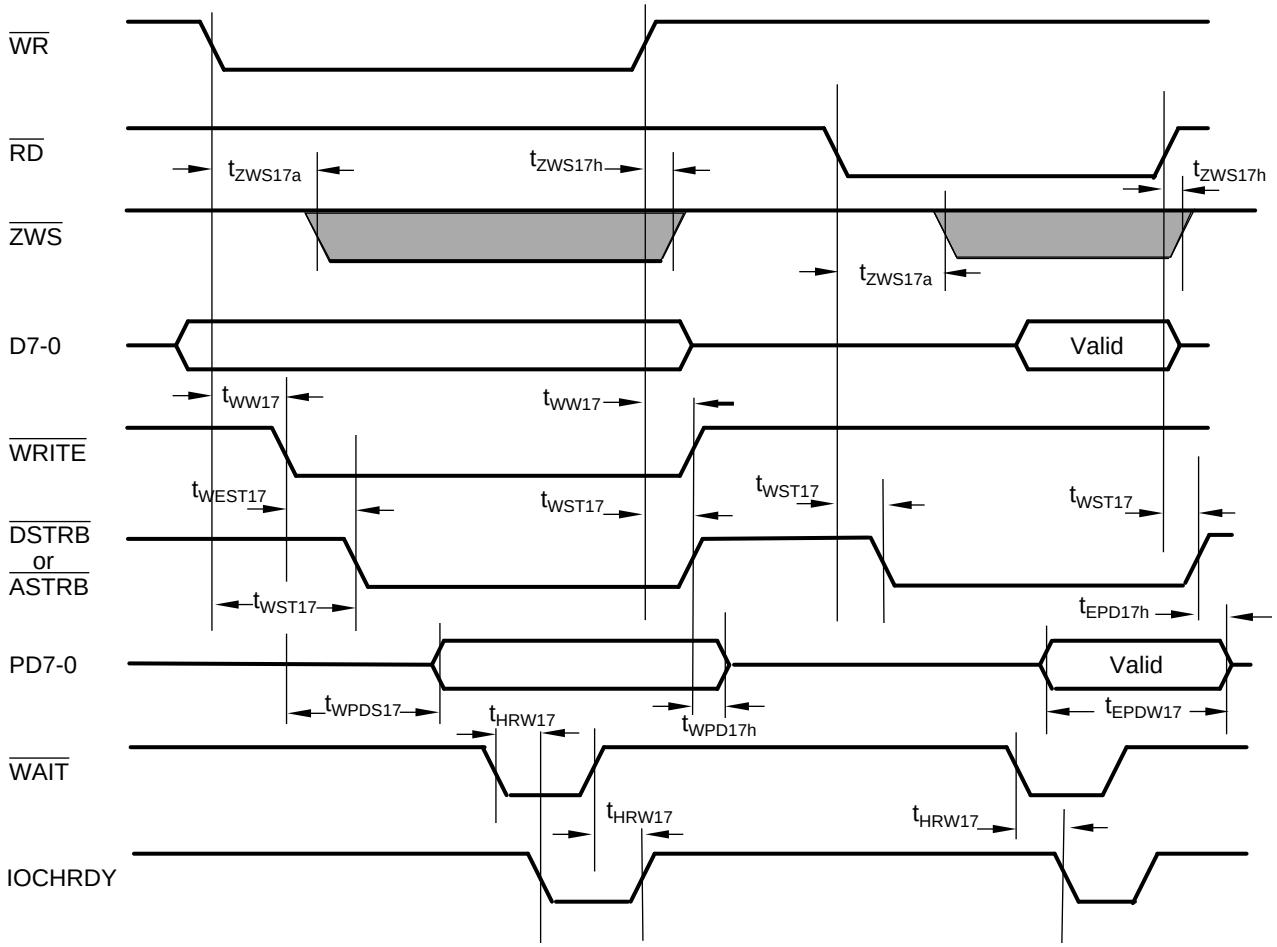


FIGURE 13-24. Enhanced Parallel Port 1.7 Timing

13.3.18 Enhanced Parallel Port 1.9 Timing

TABLE 13-54. Enhanced Parallel Port 1.9 Timing Parameters

Symbol	Parameter	Notes	Min	Max	Unit
t_{WW19a}	$\overline{WRITE}$ Active from $\overline{WR}$ Active or $\overline{WAIT}$ Low	a		45	nsec
t_{WW19ia}	$\overline{WRITE}$ Inactive from $\overline{WAIT}$ Low			45	nsec
t_{WST19a}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active from $\overline{WR}$ or $\overline{RD}$ Active or $\overline{WAIT}$ Low	a b		65	nsec
$t_{WST19ia}$	$\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive from $\overline{WR}$ or $\overline{RD}$ High			45	nsec
t_{WEST19}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active after $\overline{WRITE}$ Active		10		nsec
t_{WPD19h}	PD7-0 Hold after $\overline{WRITE}$ Inactive		0		nsec
t_{HRW19}	IOCHRDY Active after $\overline{WR}$ or $\overline{RD}$ Active or Inactive after $\overline{WAIT}$ High			40	nsec
t_{WPDS19}	PD7-0 Valid after $\overline{WRITE}$ Active	c		15	nsec
t_{EPDW19}	PD7-0 Valid Width		80		nsec
t_{EPD19h}	PD7-0 Hold after $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive		0		nsec
t_{ZWS19a}	$\overline{ZWS}$ Valid after $\overline{WR}$ or $\overline{RD}$ Active			45	nsec
t_{ZWS19h}	$\overline{ZWS}$ Hold after $\overline{WR}$ or $\overline{RD}$ Inactive		0		nsec

a. When $\overline{WAIT}$ is low, t_{WST19a} and t_{WW19a} are measured after $\overline{WR}$ or $\overline{RD}$ becomes active; else t_{WST19a} and t_{WWa} are measured after $\overline{WAIT}$ becomes low.
b. The PC87308VUL design guarantees that $\overline{WRITE}$ will not change from low to high before $\overline{DSTRB}$, or $\overline{ASTRB}$, goes from low to high.
c. D7-0 is stable 15 nsec before $\overline{WR}$ becomes active.

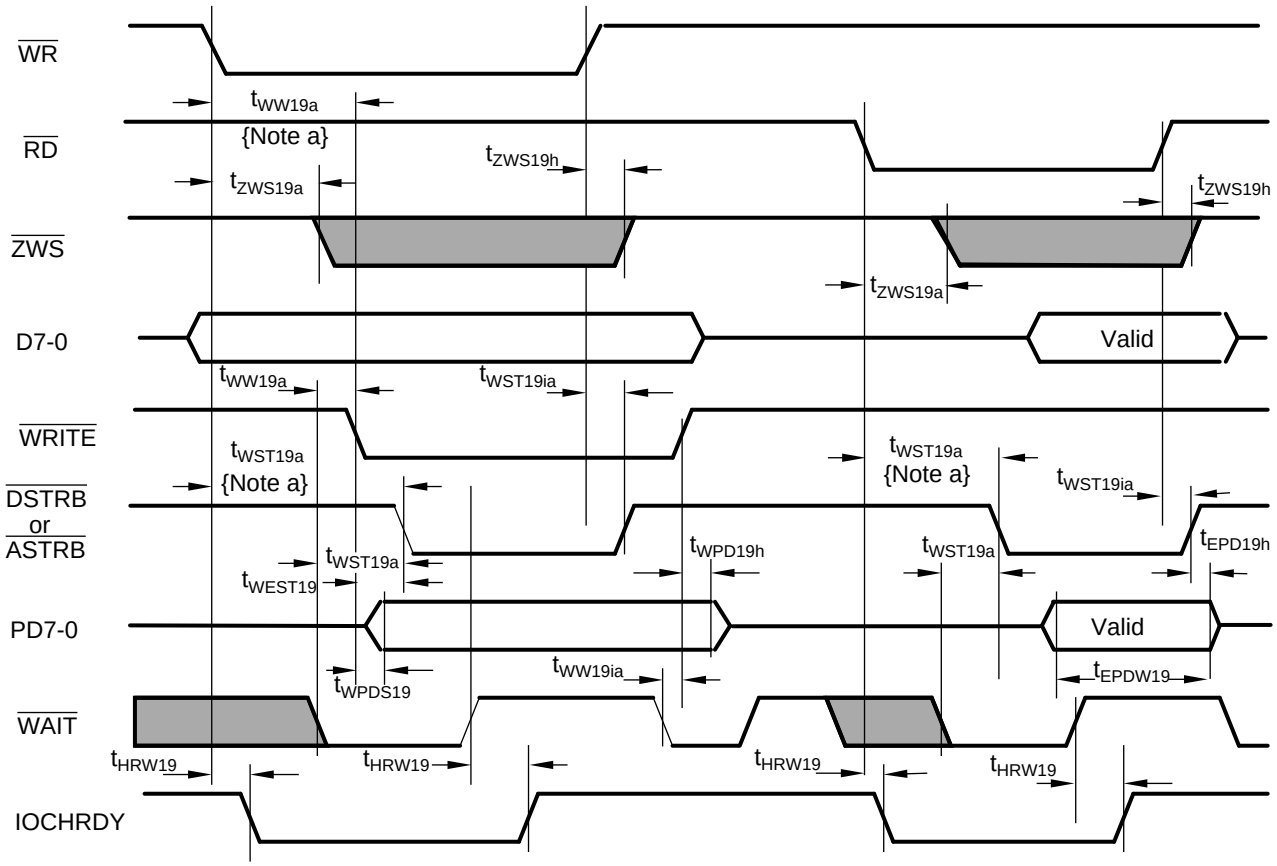


FIGURE 13-25. Enhanced Parallel Port 1.9 Timing

13.3.19 Extended Capabilities Port (ECP) Timing

TABLE 13-55. Extended Capabilities Port (ECP) Timing – Forward

Symbol	Parameter	Test Conditions	Min	Max	Unit
t_{ECDSF}	Data Setup before Strobe Active		0		nsec
t_{ECDHF}	Data Hold after BUSY		0		nsec
t_{ECLHF}	BUSY Setup after Strobe Active		75		nsec
t_{ECHHF}	Strobe Active after BUSY		0	1	sec
t_{ECHLF}	BUSY Setup after Strobe Inactive		0	35	msec
t_{ECLLF}	Strobe Active after BUSY		0		nsec

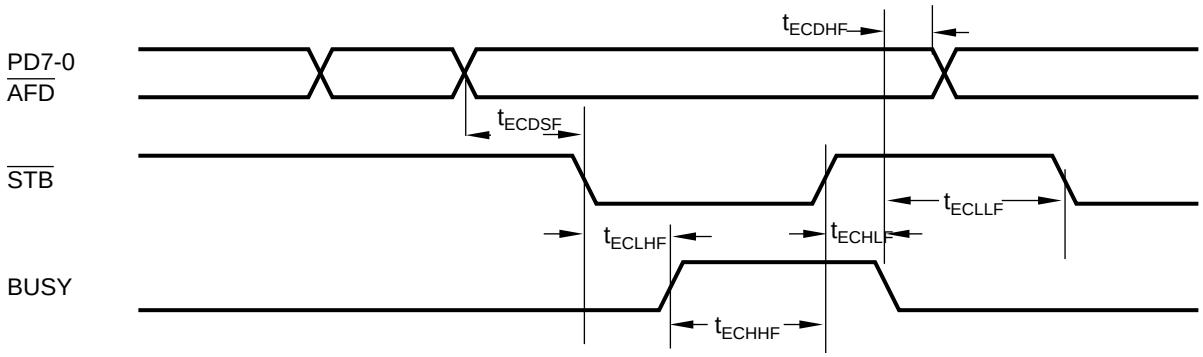


FIGURE 13-26. ECP Parallel Port Forward Timing Diagram

TABLE 13-56. Extended Capabilities Port (ECP) Timing – Backward

Symbol	Parameter	Test Conditions	Min	Max	Unit
t_{ECDSB}	Data Setup before Strobe Active		0		nsec
t_{ECDHB}	Data Hold after BUSY		0		nsec
t_{ECLHB}	BUSY Setup after Strobe Active		75		nsec
t_{ECHHB}	Strobe Active after BUSY		0	1	sec
t_{ECHLB}	BUSY Setup after Strobe Inactive		0	35	msec
t_{ECLLB}	Strobe Active after BUSY		0		nsec

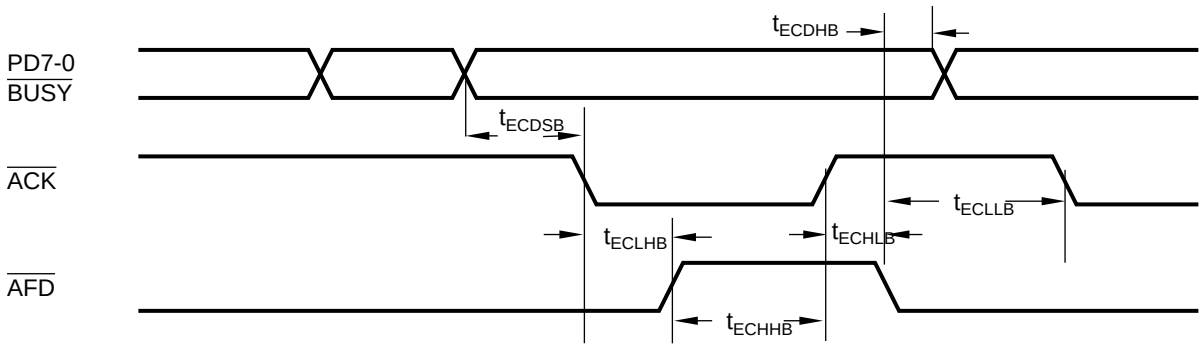


FIGURE 13-27. ECP Parallel Port Backward Timing Diagram

13.3.20 GPIO Write Timing

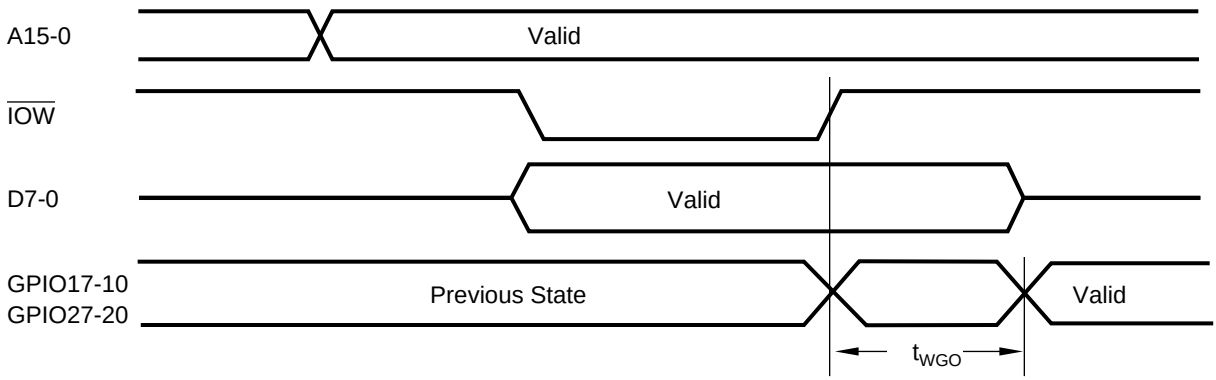


FIGURE 13-28. GPIO Write Timing Diagram

TABLE 13-57. GPIO Write Timing

Symbol	Parameter	Min	Max	Unit
t_{WGO}	Write data to GPIO update		300 [a]	nsec

a. Refer to “Microprocessor Interface Timing” on page 176 for read timing.

13.3.21 RTC Timing

TABLE 13-58. RTC Timing

Symbol	Parameter	Test Conditions	Min	Max	Unit
t_{RW}	$\overline{IOR}$ to $\overline{IRQ}$ TRI-STATE [a]			36	nsec
t_{RCI}	MR to $\overline{IRQ}$ TRI-STATE [a]			25	nsec
t_{RCL}	MR High Time		100		µsec
t_{VMR}	V_{CC} (4.5V) to MR [a]		10		msec

a. Not tested. Guaranteed by design.

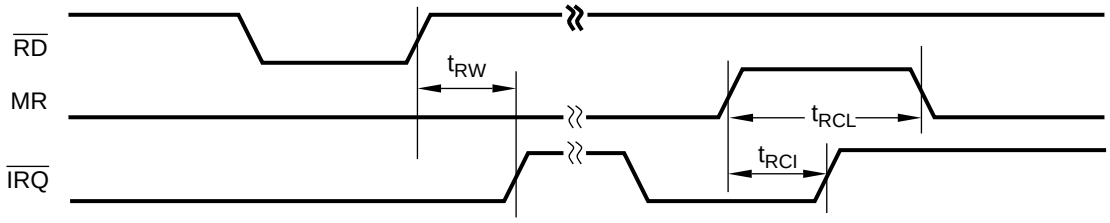


FIGURE 13-29. $\overline{IRQ}$ Release Delay

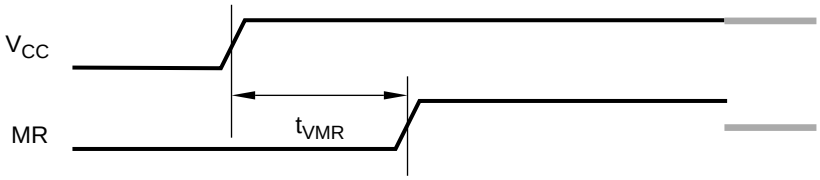


FIGURE 13-30. Master Reset (MR) Timing

13.3.22 APC Timing

TABLE 13-59. SWITCH Trigger and $\overline{\text{ONCTL}}$ Timing

Symbol	Parameter	Min	Max	Unit
t_{SWP}	SWITCH Pulse Width [a]	16		msec
t_{SWE}	Delay from SWITCH Events to $\overline{\text{ONCTL}}$, and from SWITCH Off Event to $\overline{\text{POR}}$ [a]	14	16	msec
t_{PORW}	$\overline{\text{POR}}$ Pulse Width (Edge Mode)	15	46	µsec
t_{PRL}	Delay from APCR1 Write to $\overline{\text{POR}}$ Inactive (Level Mode) [a]		25	nsec

a. Not tested. Guaranteed by design.

:

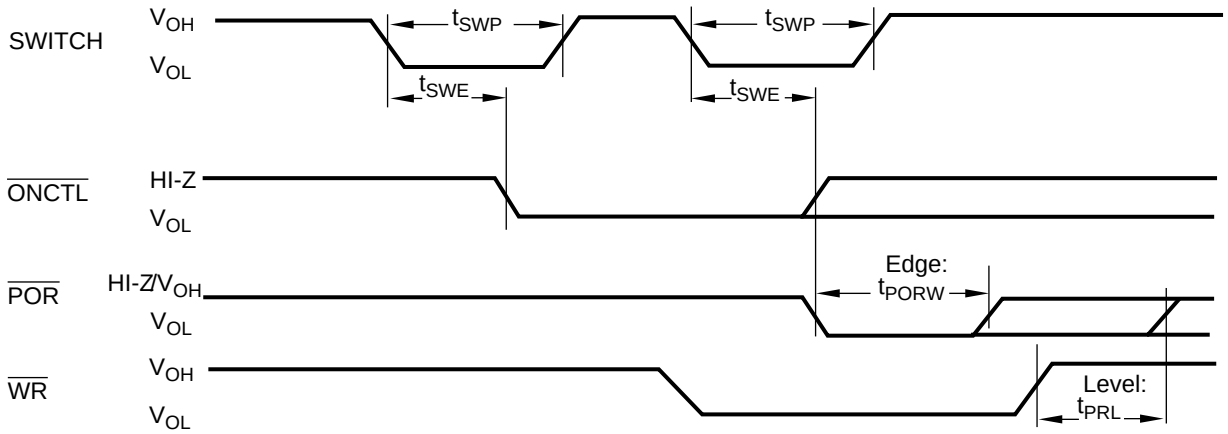


FIGURE 13-31. SWITCH Trigger and $\overline{\text{ONCTL}}$ Timing

TABLE 13-60. $\overline{\text{RI}}$ Trigger and $\overline{\text{ONCTL}}$ Timing

Symbol	Parameter	Min	Max	Unit
t_{RIO}	Delay from $\overline{\text{RI2,1}}$ to $\overline{\text{ONCTL}}$		25	nsec
t_{RIW}	$\overline{\text{RI}}$ width	10	-	nsec

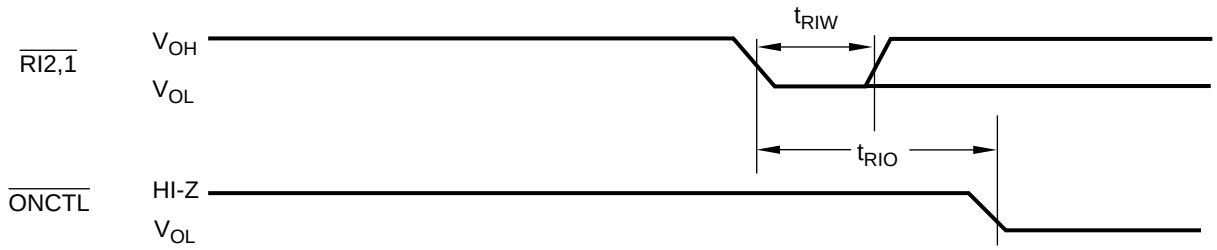


FIGURE 13-32. $\overline{\text{RI}}$ Trigger and $\overline{\text{ONCTL}}$ Timing

TABLE 13-61. $\overline{\text{RING}}$ Trigger and $\overline{\text{ONCTL}}$ Timing

Symbol	Parameter	Min	Max	Unit
t_{RPO}	Delay from $\overline{\text{RING}}$ Pulse to $\overline{\text{ONCTL}}$		25	nsec
t_{RTO}	Delay from $\overline{\text{RING}}$ Pulse Train to $\overline{\text{ONCTL}}$ [a]	0.125	0.190	sec
t_{RINW}	$\overline{\text{RING}}$ Width (High and Low Time), Single Pulse Mode	10		nsec
	$\overline{\text{RING}}$ Width (High and Low Time), Pulse Train Mode	50		µsec

a. Not tested. Guaranteed by design.

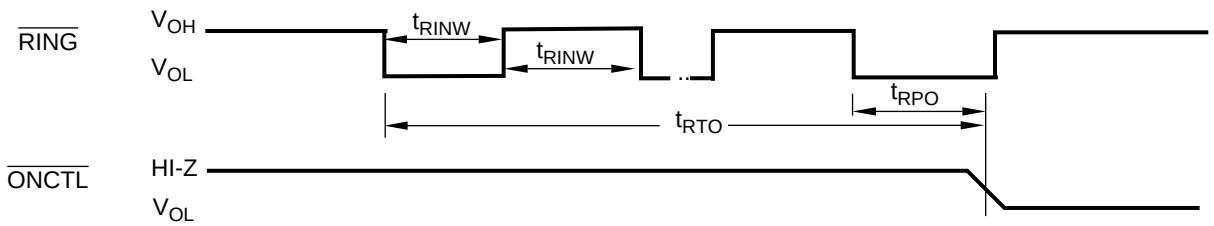


FIGURE 13-33. $\overline{\text{RING}}$ Trigger and $\overline{\text{ONCTL}}$ Timing

13.3.23 Chip Select Timing

TABLE 13-62. Chip Select Timing

Symbol	Parameter	Min	Max	Unit
t_{CE}	Delay from Command to Enable Chip Select	0	25	nsec
t_{CD}	Delay from Command to Disable Chip Select	0	25	nsec

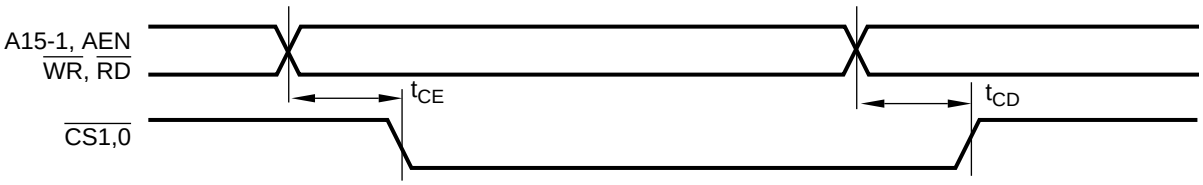


FIGURE 13-34. Chip Select Timing

Glossary

11-bit address mode
In this mode, the PC87308VUL decodes address lines A0-A10, A11-A15 are masked to 1, and UART2 is a fully featured 16550 UART. The mode is configured during reset, via CFG0 strap pin.

16-bit address mode
In this mode, the PC87308VUL decodes address lines A0-A15 and UART2 is a 16550 UART with SIN2/SOUT2 interface signals only. The mode is configured during reset, via CFG0 strap pin.

ADDR
Address Register of the parallel port in EPP modes. (Logical device 4, offset 03h.)

AFIFO
Address FIFO for the parallel port in Extended Capabilities Port (ECP) mode 011. (Logical device 4, offset 000h.)

APC
Advanced Power Control.

APCR1 and APCR2
APC control registers 1 and 2. (Logical device 2, offsets 40h and 41h, respectively.)

APSR
Advanced Power Control (APC) status register. (Logical device 2, offset 42h.)

ASCR
Auxiliary Status Register for UARTs. (Logical devices 5 and 6, bank 0, offset 07h.)

ASK-IR
Amplitude Shift Keying Infrared.

BFPLR
Beginning Flags and Preamble Length Register for UARTs. (Logical devices 5 and 6, bank 6, offset 04h.)

BGD(H) and BGD(L)
Baud rate Generator Divisor buffer (High and Low bytes) for UARTs. (Logical devices 5 and 6, bank 1, offsets 01h and 00h, respectively.)

BSR
Bank Selection Register for UARTs. (Logical devices 5 and 6, all banks, offset 03h.)

CCR
Configuration Control Register of the Floppy Disk Controller (FDC).

CFIFO
Parallel port data FIFO in Extended Capabilities Port (ECP) mode 010. (Logical device 4, offset 400h.)

CNFGA and CNFGB
Configuration registers A and B for the parallel port in Extended Capabilities Port (ECP) mode 111. (Logical device 4, offsets 400h and 401h, respectively.)

Confg0
See PP Confg0.

Consumer-IR Mode
This UART mode supports all four protocols currently used in remote-controlled home entertainment equipment. Also called TV-Remote mode.

Control0, Control2 and Control4
Internal configuration registers of the parallel port in Extended Capabilities Port (ECP) modes. (Logical device 4, second level offsets 00h, 02h and 04h.)

CSN
Card Select Number register - an 8-bit register with a unique value that identifies an ISA card.

CRA, CRB, CRC, CRD
Control Registers of the Real-Time Clock (RTC). (Logical device 2, offsets 0Ah, 0B, 0C and 0D, respectively.)

CTR
Control Register of the parallel port in SPP modes. (Logical device 4, offset 02h.)

DASK-IR
Digital Amplitude Shift Keying Infrared.

Data
The Data register contains the data in the register indicated by the corresponding Index register.

DATA0, DATA1, DATA2 and DATA3
Data Registers of the parallel port in EPP modes. (Logical device 4, offsets 04h, 05h, 06h and 07h, respectively.)

DATAR
Data Register for the parallel port in Extended Capability Port (ECP) modes 000 and 001. (Logical device 4, offset 000h.)

DCR
Data Control Register for the parallel port in Extended Capabilities Port (ECP) modes. (Logical device 4, offset 002h.)

Device
Any circuit that performs a specific function, such as a parallel port.

DFIFO
ECP Data FIFO in Extended Capabilities Port (ECP) mode 011. (Logical device 4, offset 400h.)

DIR
Digital Input Register of the Floppy Disk Controller (FDC).

DOR
Digital Output Register of the Floppy Disk Controller (FDC).

DSR
Data rate Select Register of the Floppy Disk Controller (FDC) (logical device 3) and the Data Status Register in Extended Capabilities Port (ECP) modes (logical device 4, offset 001h).

DTR
Data Register of the parallel port in SPP or EPP modes. (Logical device 4, offset 00h.)

EAR
Extended Auxiliary Register of the parallel port in Extended Capabilities Port (ECP) modes. (Logical device 4, offset 405h.)

ECP
Extended Capabilities Port.

ECR
Extended Control Register for the parallel port in Extended Capabilities Port (ECP) modes. (Logical device 4, offset 402h.)

EDR
Extended Data Register for the parallel port in extended Capabilities Port (ECP) modes. (Logical device 4, offset 404h.).

EIR
Extended Index Register of the parallel port Extended Capabilities Port (ECP) modes (logical device 4, offset 403h) or Event Identification Register for UARTs (logical devices 5 and 6, bank 0, offset 02h).

EPP
Enhanced Parallel Port.

EXCR1 and EXCR2
Extended Control Registers 1 and 2 for UART2.

FCR
The FIFO Control Register for UARTs. (Logical devices 5 and 6, bank 0, offset 02h.)

FDC
Floppy Disk Controller.

FDD
Floppy Disk Drive.

FER1 and FER2
Function Enable Registers of the Power Management device (Logical device 8, offsets 00h and 01h, respectively.).

FIFO
Data register (FIFO queue) of the Floppy Disk Controller (FDC).

FRM_ST
Frame Status register for UART2.

GPIO
General Purpose I/O - I/O pins available for general use.

IER
The Interrupt Enable Register for UARTs. (Logical devices 5 and 6, bank 0, offset 01h.)

Index
The Index register is a pointer that is used to address other registers.

IR
Infrared.

IRCFG1, IRCFG2, IRCFG3 and IRCFG4
Infrared module Configuration registers for UART2.)

IRCR1, IRCR2 and IRCR3
Infrared module Control Registers 1, 2 and 3 for UART2.

IrDA
Infrared Data Association.

IRQ
Interrupt Request.

IRRXDC
Infrared Receiver Demodulator Control register for UART2.

IRTXMC
Infrared Transmitter Modulator Control register for UART2.

ISA
Industry Standard Architecture for the PC bus.

LBGD(H) and LBGD(L)
Legacy Baud rate Generator Divisor port (High and Low bytes) for the UART2.

LCR
Line Control Register for UARTs. (Logical devices 5 and 6, all banks, offset 03h.)

Legacy
Usually refers to older devices or systems that are not Plug and Play compatible.

Legacy Mode
In this mode, the interrupts and the base addresses of the FDC, UARTs, KBC, RTC and the parallel port of the PC87308VUL are configured as in earlier SuperI/O chips.

LFSR
The Linear Feedback Shift Register. In Plug and Play mode, this register is used to prepare the chip for operation in Plug and Play (PnP) mode.

LSB
Least Significant Byte or Bit.

LSR
Line Status Register for UARTs. (Logical devices 5 and 6, bank 0, offset 05h.)

MCR
Modem Control Register for UARTs. (Logical devices 5 and 6, bank 0, offset 04h.)

MIR_PW
MIR Pulse Width control for UART2. (Logical devices 5, bank 6, offset 01h.)

MSB
Most Significant Byte or Bit.

MSR
Main Status Register of the Floppy Disk Controller (FDC) (Logical device 3) or Modem Status Register for UARTs (Logical devices 5 and 6, bank 0, offset 01h).

P_BGDH and P_BGDL
Pipeline Baud rate Generator Divisor buffer (High and Low bytes) for UART2. (Logical devices 5, bank 5, offsets 01h and 00h, respectively.)

PIO
Programmable Input/Output.

P_MDR
Pipeline Mode Register for UART2. (Logical devices 5, bank 5, offset 02h.)

Plug and Play
A design philosophy and a set of specifications that describe hardware and software changes to the PC and its peripherals that automatically identify and arbitrate resource requirements among all devices and buses on the system. Plug and Play is sometimes abbreviated as PnP.

PM
Power Management.

PMC1, PMC2 and PMC3
Power Management Control registers of logical device 8.

PnP
Sometimes used to indicate Plug and Play.

PnP Mode
In this mode, the interrupts, the DMA channels and the base address of the FDC, UARTs, KBC, RTC, GPIO, APC and the Parallel Port of the PC87308VUL are fully Plug and Play.

PP Confg0
Internal configuration register of the Parallel Port in Extended Capabilities Port (ECP) modes. (Logical device 4, second level offset 05h.)

ppm
Parts per million.

PPM
Parallel Port Multiplexor or Multiplexed.

Precompensation
Also called write precompensation, is a way of preconditioning the WDATA output signal to adjust for the effects of bit shift on the data as it is written to the disk surface.

RCCFG
Consumer Remote Control Configuration register for UART2. (Logical devices 5, bank 7, offset 02h.)

RFRL(H) and RFRL(L)
Received Frame Length at bottom of status FIFO (High and Low bytes) for UART2. (Logical devices 5, Bank 5, offsets 07h and 06h, respectively.)

RFRML(H) and RFRML(L)
Reception Frame Maximum Length (High and Low bytes) for UART2. (Logical devices 5, Bank 4, offsets 07h and 06h, respectively.)

RFRCC(H) and RFRCC(L)
Reception Frame Current Count (High and Low bytes) for UART2. (Logical devices 5, bank 4, offsets 07h and 06h, respectively.)

RLC
Run Length Count byte for parallel ports.

RLE
Run Length Expander for parallel ports.

RLR
RAM Lock Register for Advanced Power Control (APC). (Logical device 2, offset 47h.)

RTC
The Real-Time Clock.

RXFLV
Reception FIFO Level for UART2. (Logical devices 5, bank 2, offset 07h.)

SCR
Scratch Register for UARTs. (Logical devices 5 and 6, bank 0, offset 07h.)

SH_FCR
Shadow of the FIFO Control Register (FCR) for UART2. (Logical devices 5, bank 3, offset 02h.)

SH_LCR
Shadow of the Line Control Register (LCR) for UART2. (Logical devices 5, bank 3, offset 01h.)

Sharp-IR
Sharp Infrared.

Sharp-IR Mode
In this mode, the PC87308VUL supports a Sharp Infrared interface.

SIO
SuperI/O, sometimes used to refer to a chip that has SuperI/O capabilities, e.g., the PC87308VUL chip.

SIR
Serial Infrared.

SIR_PW
SIR Pulse Width control for UART2. (Logical devices 5, bank 6, offset 02h.)

SPP
The Standard Parallel Port configuration of the Parallel Port device (Logical device 4) supports the Compatible SPP mode and the Extended PP mode.

SRA and SRB
Status Registers A and B of the Floppy Disk Controller (FDC).

ST0, ST1, ST2 and ST3
Status registers 0, 1, 2 and 3 of the Floppy Disk Controller (FDC).

STR
Status Register of the parallel port in SPP modes. (Logical device 4, offset 01h.)

TDR
Tape Drive Register of the Floppy Disk Controller (FDC).

TFIFO
Test FIFO for the parallel port in Extended Capabilities Port (ECP) mode 110. (Logical device 4, offset 400h.)

TFRL(H) and TFRL(L)
Transmission Frame Length (High and Low bytes) for UART2. (Logical devices 5, bank 4, offsets 05h and 04h, respectively.)

TFRCC(H) and TFRCC(L)
Transmission Frame Current Count (High and Low bytes) for UART2. (Logical devices 5, bank 4, offsets 05h and 40,h respectively.)

TMRH and TMRL
Interval Timer (High and Low bytes) for UART2. (Logical devices 5, bank 5, offsets 01h and 00h, respectively.)

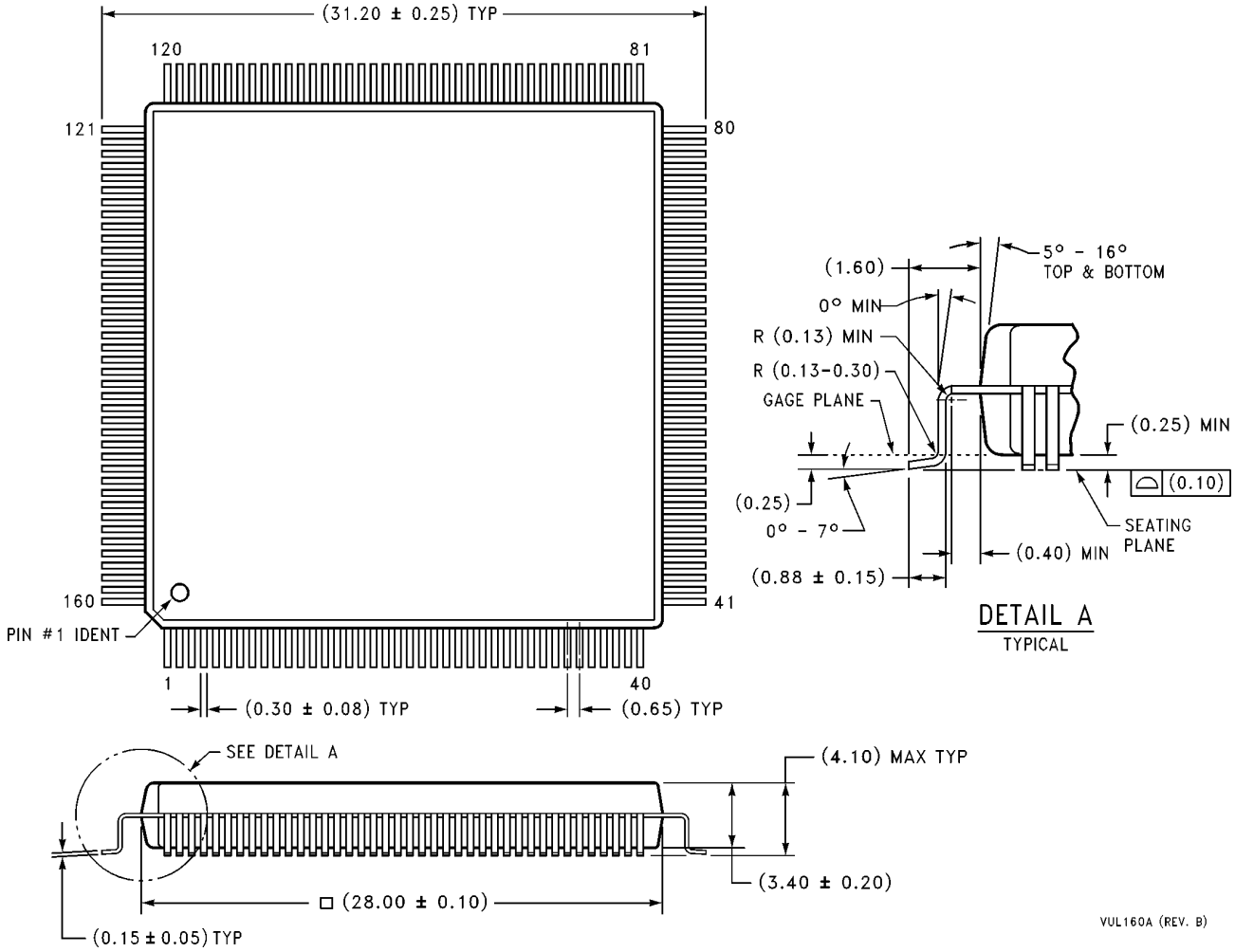
TV-Remote Mode
See Consumer-IR mode.

TXFLV
Transmission FIFO Level for UART2. (Logical devices 5, bank 2, offset 06h.)

UART, UART1 and UART2
Universal Asynchronous Receiver Transmitter. The PC87308VUL supports two UARTs, UART1 and UART2. They are identical, with the exception that UART2 includes infrared support.

XDB
X-Bus Data Buffer.

Physical Dimensions millimeters



PlasticQuad Flatpack (PQFP), EIAJ
Order Number PC87308VUL
NS Package Number VUL160A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Dr.
P.O. Box 58090
Santa Clara,
CA 95052-8090
Tel: +1 (800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256
Furstenfeldbruck,
Germany
Tel: (81 41) 35-0
Telex: 527649
Fax: (81 41) 35-1

National Semiconductor Japan Ltd.
URD-KIBA Building
2-17-16, Kiba, Koutou-Ku
Tokyo 135, Japan
Tel: +81 3 5620-6170
Fax: +81 3 5620-6179

National Semiconductor Hong Kong Ltd.
13 Floor, Straight Block
Ocean Centre,
5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1601
Telex: 51292 NSHKL
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda
Franco 120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
16 Business Park Dr.
Notting Hill, VIC 3168
Australia
Tel: (3) 558-9999
Fax: (3) 558-9998